

PJQ65702U3-AU

100V N-Channel Enhancement Mode MOSFET

Voltage

100 V

Current

340 A

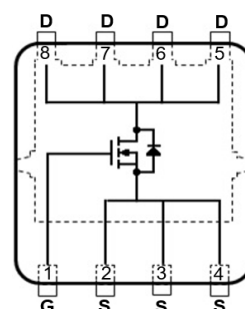
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@50A < 1.7m\Omega$
- Standard Level Drive
- 100% UIS tested
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : PDFN8080-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.2 grams

PDFN8080-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^{\circ}C$	I_D	340	A
	$T_C=100^{\circ}C$		240	
Pulsed Drain Current ^(Note 1)	$T_C=25^{\circ}C$	I_{DM}	1360	
Power Dissipation	$T_C=25^{\circ}C$	P_D	395	W
	$T_C=100^{\circ}C$		197	
Continuous Drain Current ^(Note 4)	$T_A=25^{\circ}C$	I_D	37	A
	$T_A=70^{\circ}C$		31	
Power Dissipation	$T_A=25^{\circ}C$	P_D	4.7	W
	$T_A=70^{\circ}C$		3.3	
Single Pulse Avalanche Current ^(Note 5)		I_{AS}	45	A
Single Pulse Avalanche Energy ^(Note 5)		E_{AS}	1013	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^{\circ}C$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	0.38	$^{\circ}C/W$
	Junction to Ambient	$R_{\theta JA}$	32	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	100	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =1mA	2	-	3.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =50A	-	1.35	1.7	mΩ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 5)						
Total Gate Charge	Q _g	V _{DS} =50V, I _D =50A, V _{GS} =10V	-	239	310	nC
Gate-Source Charge	Q _{gs}		-	57	-	
Gate-Drain Charge	Q _{gd}		-	34	-	
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	16934	22000	pF
Output Capacitance	C _{oss}		-	3778	5000	
Reverse Transfer Capacitance	C _{rss}		-	90	180	
Gate resistance	R _g	f=1MHz	-	0.85	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} =50V, I _D =50A, V _{GS} =10V, R _G =3Ω (Note 2)	-	52	-	ns
Turn-On Rise Time	t _r		-	56	-	
Turn-Off Delay Time	t _{d(off)}		-	103	-	
Turn-Off Fall Time	t _f		-	44	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25°C (Package Limit)	-	-	340	A
Pulsed Diode Forward Current	I _{SM}		-	-	1360	
Diode Forward Voltage	V _{SD}	I _S =50A, V _{GS} =0V	-	0.8	1.3	V
Reverse Recovery Time	T _{rr}	V _{DD} =50V,V _{GS} =0V,	-	135	-	ns
Reverse Recovery Charge	Q _{rr}	I _S =30A,dI _S /dt=100A/us	-	460	-	nC

NOTES :

1. Pulse width≤100us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=0.38°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance. Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5,-7) PCB is vertical in still air.
5. E_{AS} is calculated based on the condition of L=1mH, I_{AS}=45A, V_{DD}=50V, V_{GS}=10V. 100% test at L=0.5mH, I_{AS}=46A in production.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

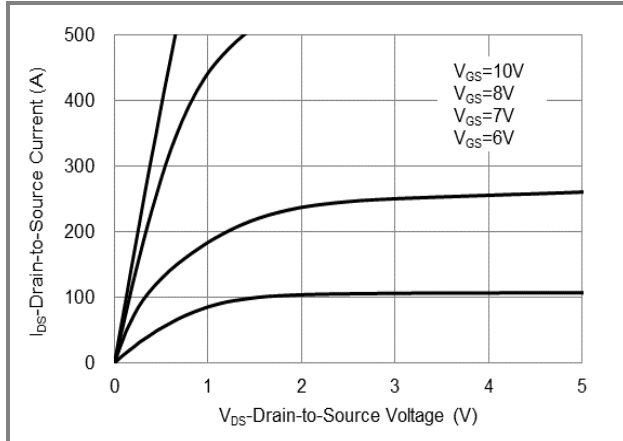


Fig.1 On-Region Characteristics

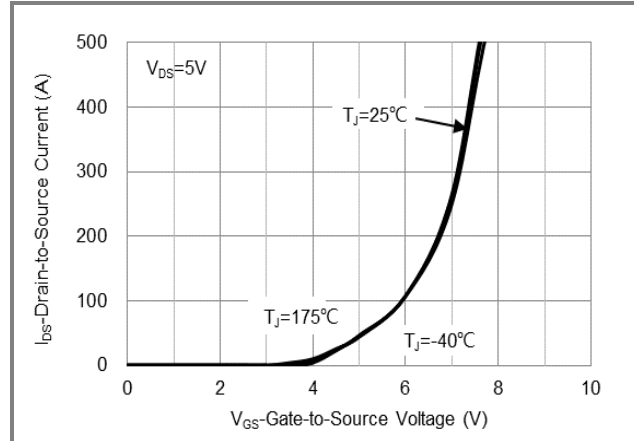


Fig.2 Transfer Characteristics

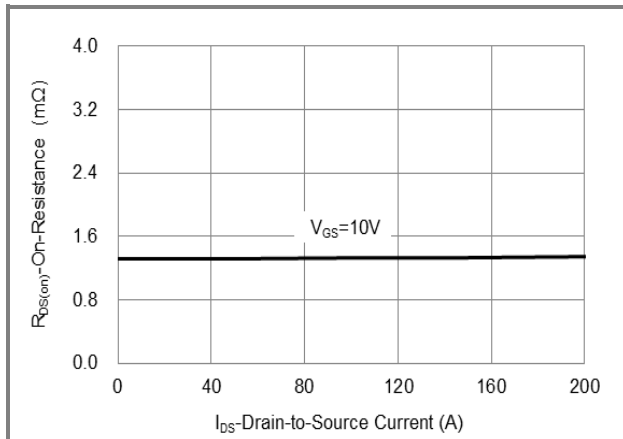


Fig.3 On-Resistance vs. Drain Current

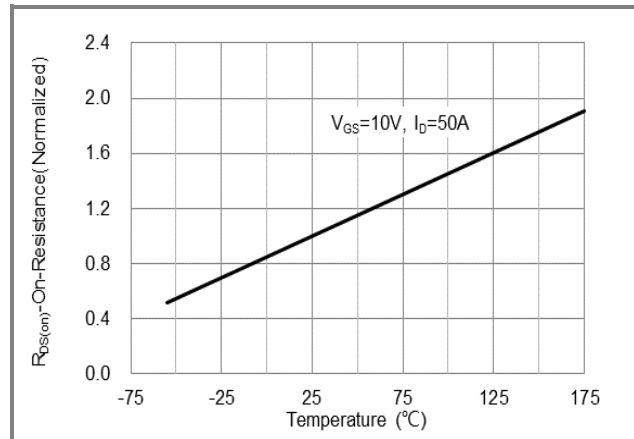


Fig.4 On-Resistance vs. Junction temperature

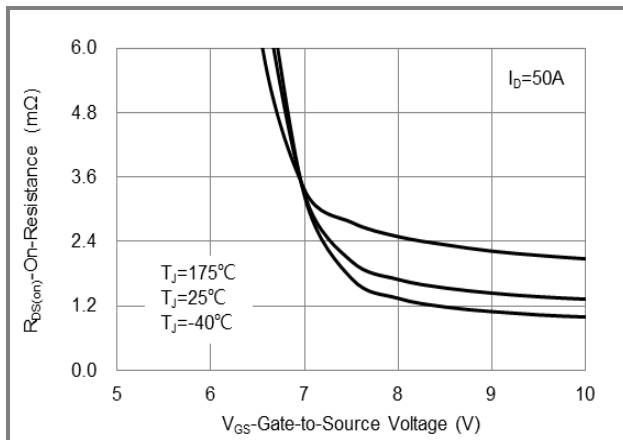


Fig.5 On-Resistance Variation with V_{GS}

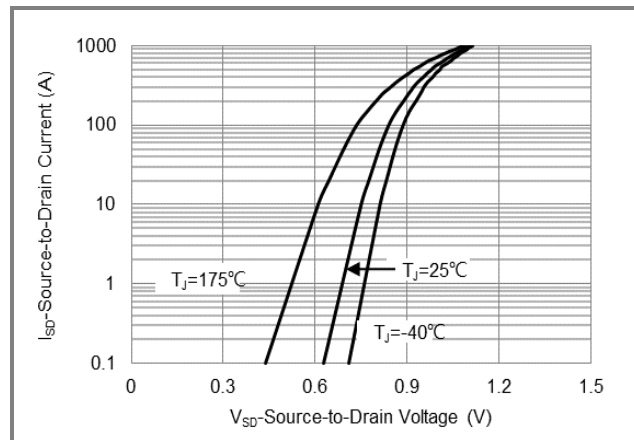
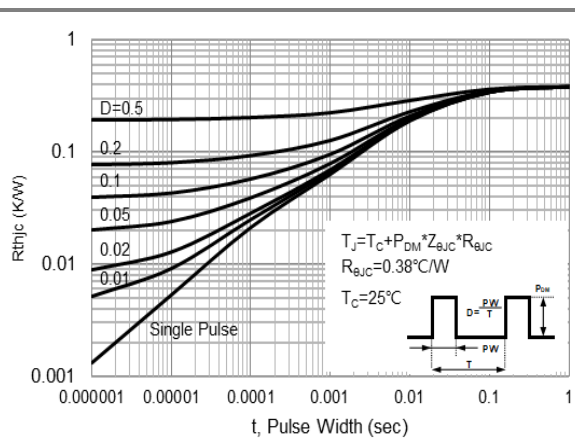
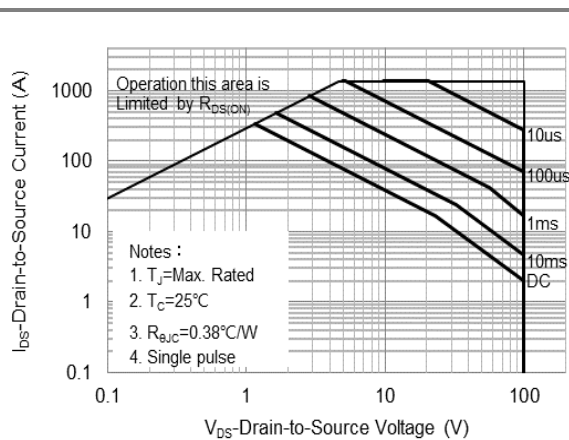
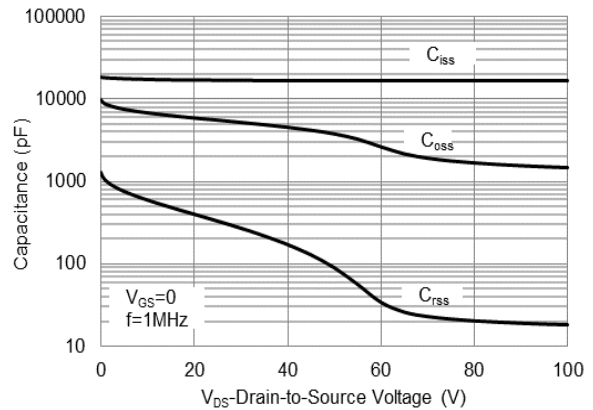
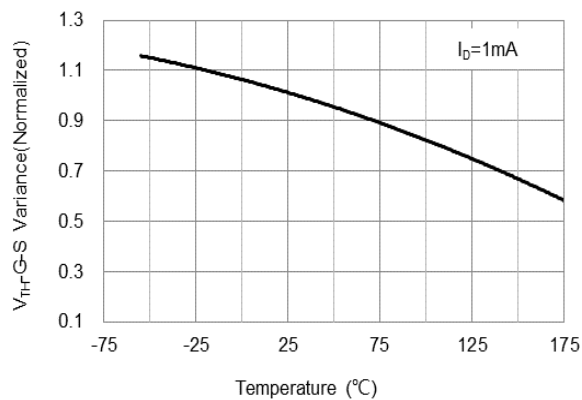
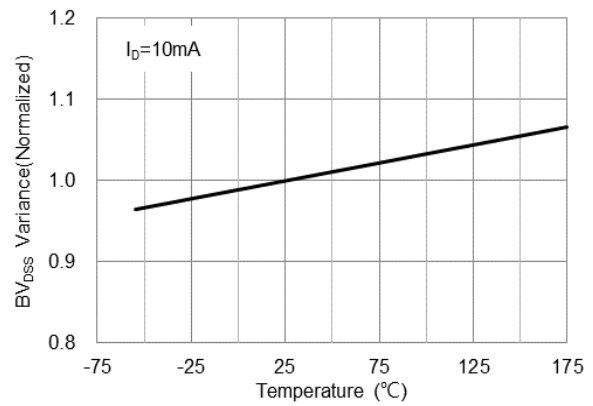
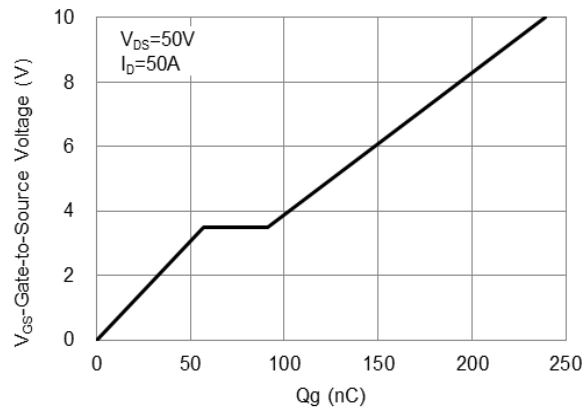


Fig.6 Source-Drain Diode Forward Voltage

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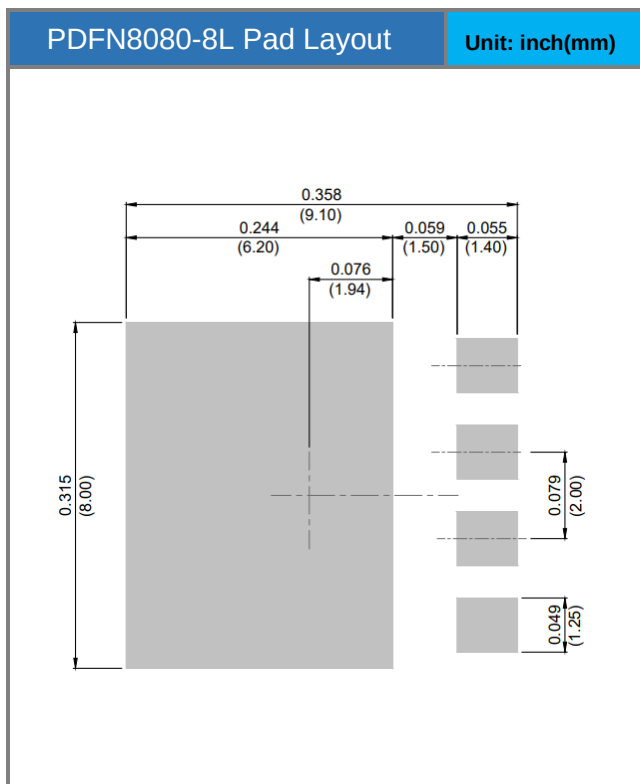
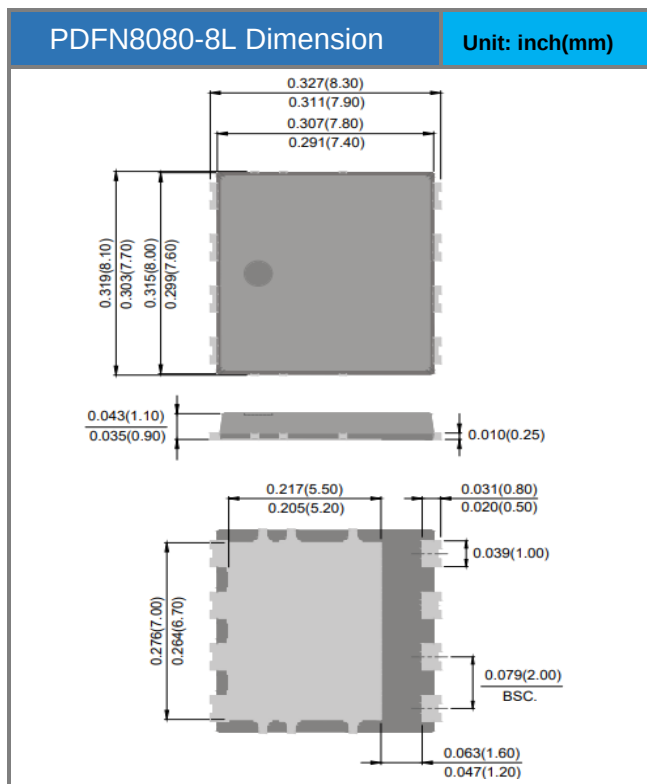


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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ65702U3-AU	PDFN8080-8L	3K pcs / 13" reel	65702U3

Packaging Information & Mounting Pad Layout



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