

PS1A1M-W62

Low Capacitance ESD Protection

Voltage

24 V

Features

- IEC61000-4-2(ESD) : $\pm 30\text{kV}$ Air, $\pm 30\text{kV}$ Contact
- IEC61000-4-5(Lightning) : 20A (8/20 μs)
- Ultra-Low Capacitance : 3.6pF
- Low leakage current, maximum of 1 μA at rated voltage
- Low clamping voltage
- Pb-Free/Halogen Free/BFR Free and RoHS Compliant
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

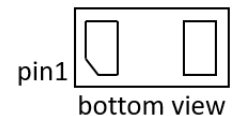
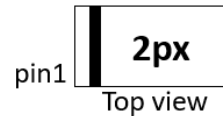
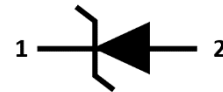
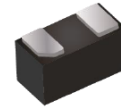
Mechanical Data

- Case : DFN1006-2L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0006 grams

Applications

- USB 2.0
- Type-C connector CC/SBU
- Consumer electronics

DFN1006-2L



Part Marking	Parameter
2px	2p = Marking Code x = Tracking Code

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
ESD IEC61000-4-2(Air)	V _{ESD}	± 30	kV
ESD IEC61000-4-2(Contact)		± 30	
Operating Junction Temperature Range	T _J	-55~125	°C
Storage Temperature Range	T _{STG}	-55~150	°C

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Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reverse Stand-Off Voltage ^(Note 2)	V_{RWM}	Pin1 to Pin2	-	-	24	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 10\mu\text{A}$, Pin1 to Pin2	25	-	-	V
Forward Voltage	V_F	$I_F = 15\text{mA}$, Pin2 to Pin1	-	1	-	V
Reverse Leakage Current	I_R	$V_{RWM} = 24\text{V}$, Pin1 to Pin2	-	0.5	1	μA
Surge Clamping Voltage (8/20us)	V_{CL}	$I_{PP} = 20\text{A}$, Pin1 to Pin2	-	4.5	5.5	V
Clamping Voltage TLP ($t_{period}=100\text{ns}$, $t_r=1\text{ns}$) ^(Note 3)	V_C	$I_{TLP} = 16\text{A}$, Pin1 to Pin2	-	3	-	V
Off State Junction Capacitance (Note 4)	C_J	$V_R=0\text{V}$, $f=1\text{MHz}$, Pin1 to Pin2	-	3.6	3.9	pF

NOTES :

1. Mounted on a FR4 PCB, Single-sided copper, mini pad.
2. A transient suppressor is selected according to the working peak reverse voltage(V_{RWM}), which should be equal to or greater than the DC or continuous peak operation voltage level.
3. Testing using Transmission Line Pulse (TLP) conditions: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$.
4. This parameter is guaranteed by design.
5. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid the ESD protection device maintain in snap-back state after exceeding breakdown voltage.

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TYPICAL CHARACTERISTIC CURVES

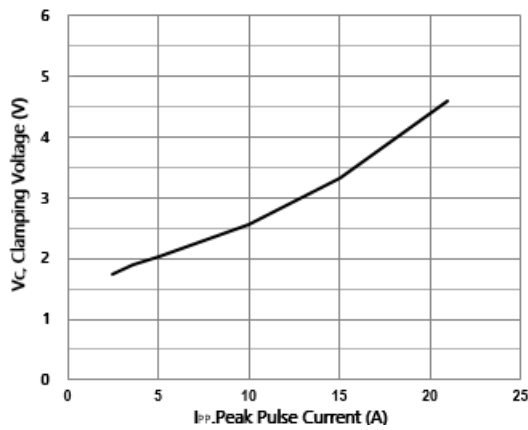


Fig.1 Typical Peak Clamping Voltage

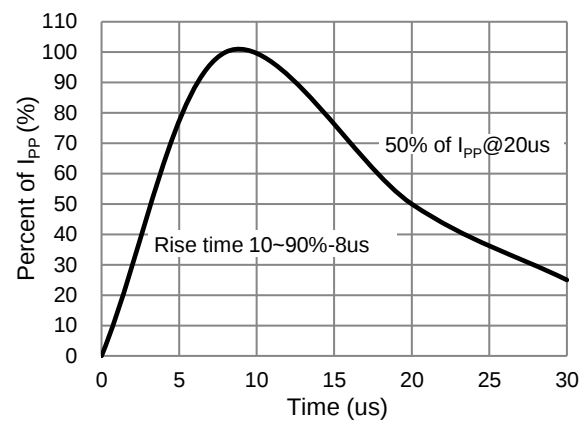


Fig.2 Pulse Waveform

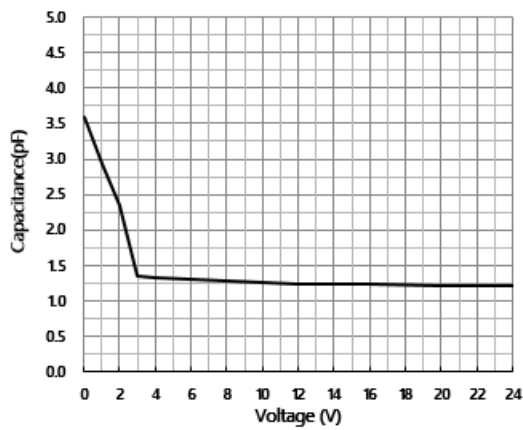


Fig.3 Typical Junction Capacitance

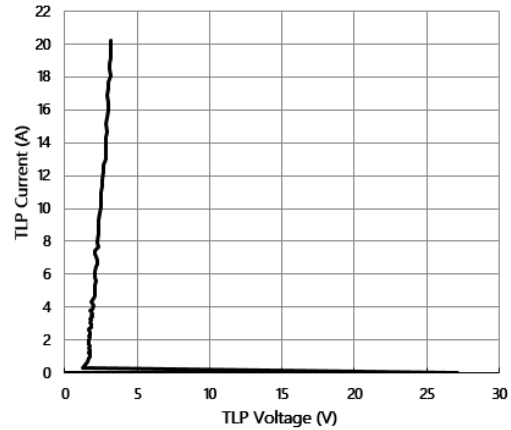


Fig.4 Positive TLP Measurement

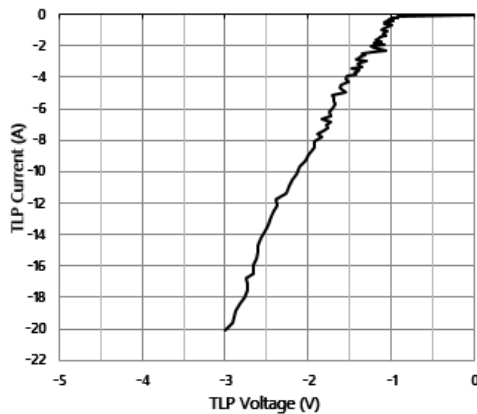


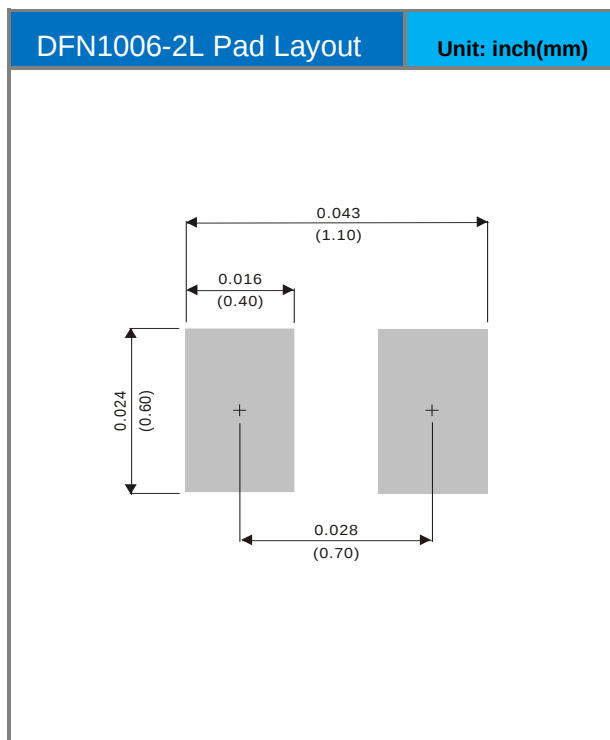
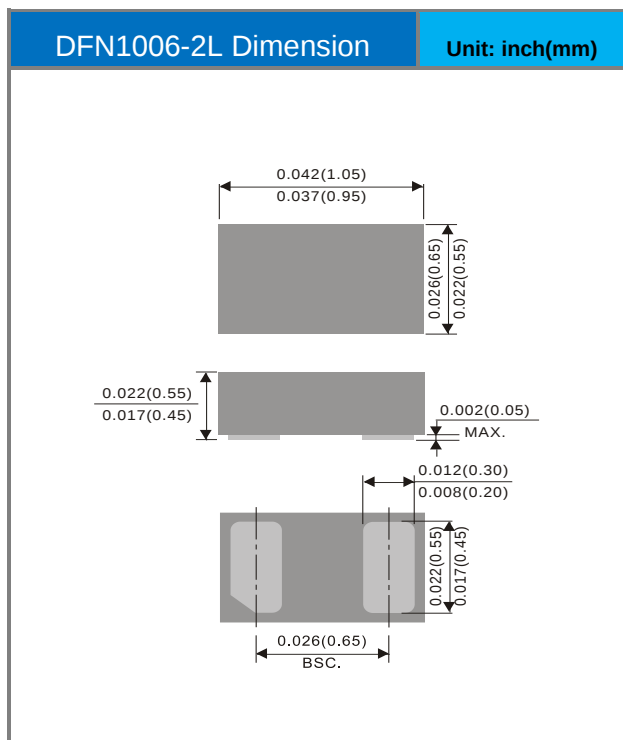
Fig.5 Negative TLP Measurement

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PS1A1M-W62	DFN1006-2L	10K pcs / 7" reel	2p

Packaging Information & Mounting Pad Layout



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