

# PJQ55802-AU

## 80V N-Channel Enhancement Mode MOSFET

**Voltage**

**80 V**

**Current**

**155 A**

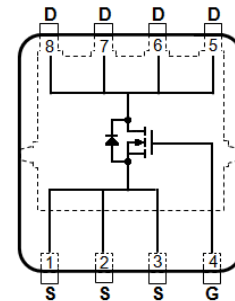
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@20A<3.3m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@7V$ ,  $I_D@10A<4m\Omega$
- Excellent FOM
- Standard Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.08 grams

DFN5060-8L



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

| PARAMETER  |                         | SYMBOL          | LIMIT    | UNITS              |
|--|-------------------------|-----------------|----------|--------------------|
| Drain-Source Voltage                               |                         | $V_{DS}$        | 80       | V                  |
| Gate-Source Voltage                                |                         | $V_{GS}$        | $\pm 20$ |                    |
| Continuous Drain Current <sup>(Note 3)</sup>       | $T_C=25^\circ\text{C}$  | $I_D$           | 155      | A                  |
|  | $T_C=100^\circ\text{C}$ |                 | 110      |                    |
| Pulsed Drain Current <sup>(Note 1)</sup>           | $T_C=25^\circ\text{C}$  | $I_{DM}$        | 620      |                    |
| Power Dissipation                                  | $T_C=25^\circ\text{C}$  | $P_D$           | 160      | W                  |
|  | $T_C=100^\circ\text{C}$ |                 | 80       |                    |
| Continuous Drain Current <sup>(Note 4)</sup>       | $T_A=25^\circ\text{C}$  | $I_D$           | 22.5     | A                  |
|  | $T_A=70^\circ\text{C}$  |                 | 18.8     |                    |
| Power Dissipation                                  | $T_A=25^\circ\text{C}$  | $P_D$           | 3.3      | W                  |
|  | $T_A=70^\circ\text{C}$  |                 | 2.3      |                    |
| Single Pulse Avalanche Current <sup>(Note 5)</sup> |                         | $I_{AS}$        | 23       | A                  |
| Single Pulse Avalanche Energy <sup>(Note 5)</sup>  |                         | $E_{AS}$        | 235      | mJ                 |
| Operating Junction and Storage Temperature Range   |                         | $T_J, T_{STG}$  | -55~175  | $^\circ\text{C}$   |
| Thermal Resistance <sup>(Note 4)</sup>             | Junction to Case        | $R_{\theta JC}$ | 0.94     | $^\circ\text{C/W}$ |
|  | Junction to Ambient     | $R_{\theta JA}$ | 45       |                    |

# PJQ55802-AU

## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

| PARAMETER                        | SYMBOL              | TEST CONDITION   | MIN. | TYP. | MAX. | UNITS |
|----------------------------------|---------------------|--|------|------|------|-------|
| Static                           |                     |  |      |      |      |       |
| Drain-Source Breakdown Voltage   | BV <sub>DSS</sub>   | V <sub>GS</sub> =0V, I <sub>D</sub> =250uA   | 80   | -    | -    | V     |
| Gate Threshold Voltage           | V <sub>GS(th)</sub> | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA   | 2    | 3    | 4    |       |
| Drain-Source On-State Resistance | R <sub>DS(on)</sub> | V <sub>GS</sub> =10V, I <sub>D</sub> =20A  | -    | 2.6  | 3.3  | mΩ    |
|                                  |                     | V <sub>GS</sub> =7V, I <sub>D</sub> =10A   | -    | 3.1  | 4    |       |
| Zero Gate Voltage Drain Current  | I <sub>DSS</sub>    | V <sub>DS</sub> =80V, V <sub>GS</sub> =0V  | -    | -    | 1    | uA    |
| Gate-Source Leakage Current      | I <sub>GSS</sub>    | V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V   | -    | -    | ±100 | nA    |
| Dynamic <sup>(Note 6)</sup>      |                     |  |      |      |      |       |
| Total Gate Charge                | Q <sub>g</sub>      | V <sub>DS</sub> =40V, I <sub>D</sub> =20A,<br>V <sub>GS</sub> =10V                                 | -    | 89   | 120  | nC    |
| Gate-Source Charge               | Q <sub>gs</sub>     |  | -    | 18   | -    |       |
| Gate-Drain Charge                | Q <sub>gd</sub>     |  | -    | 21   | -    |       |
| Input Capacitance                | C <sub>iss</sub>    | V <sub>DS</sub> =40V, V <sub>GS</sub> =0V,<br>f=1MHz   | -    | 5268 | 6900 | pF    |
| Output Capacitance               | C <sub>oss</sub>    |  | -    | 939  | 1400 |       |
| Reverse Transfer Capacitance     | C <sub>rss</sub>    |  | -    | 25   | 50   |       |
| Gate resistance                  | R <sub>g</sub>      | f=1MHz   | -    | 1.3  | -    | Ω     |
| Turn-On Delay Time               | td <sub>(on)</sub>  | V <sub>DS</sub> =40V, I <sub>D</sub> =20A,<br>V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω<br>(Note 2) | -    | 21   | -    | ns    |
| Turn-On Rise Time                | tr                  |  | -    | 23   | -    |       |
| Turn-Off Delay Time              | td <sub>(off)</sub> |  | -    | 60   | -    |       |
| Turn-Off Fall Time               | tf                  |  | -    | 22   | -    |       |
| Drain-Source Diode               |                     |  |      |      |      |       |
| Diode Forward Current            | Is                  | T <sub>C</sub> =25°C<br>(Package Limit)  | -    | -    | 155  | A     |
| Pulsed Diode Forward Current     | ISM                 |  | -    | -    | 620  |       |
| Diode Forward Voltage            | VSD                 | Is=20A, VGS=0V   | -    | 0.8  | 1.3  | V     |
| Reverse Recovery Time            | Trr                 | VDD=40V, VGS=0V,   | -    | 64   | -    | ns    |
| Reverse Recovery Charge          | Qrr                 | Is=20A, dIs/dt=100A/us   | -    | 82   | -    | nC    |

### NOTES :

- Pulse width ≤ 100us, Duty cycle ≤ 2%.
- Essentially independent of operating temperature typical characteristics.
- Chip capability with an R<sub>θJC</sub>=0.94°C/W, Package limited 120A.
- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
- E<sub>AS</sub> is calculated based on the condition of L=1mH, I<sub>AS</sub>=21.7A, V<sub>DD</sub>=30V, V<sub>GS</sub>=10V. 100% test at L=0.5mH, I<sub>AS</sub>=23A in production.
- Guaranteed by design, not subject to production testing.

## PJQ55802-AU

### TYPICAL CHARACTERISTIC CURVES

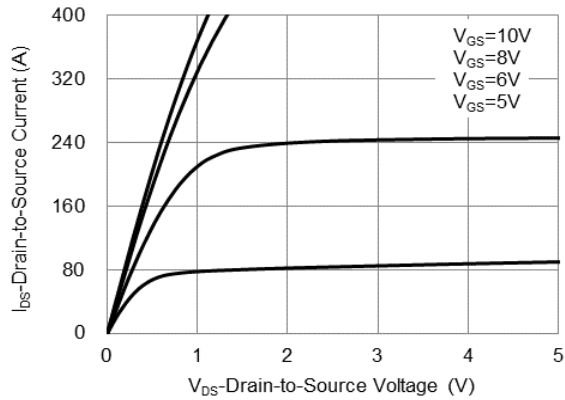


Fig.1 On-Region Characteristics

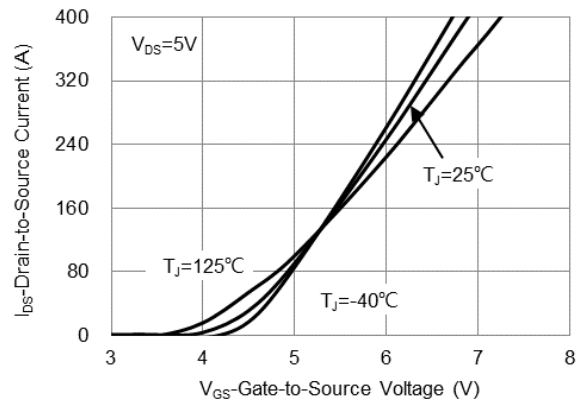


Fig.2 Transfer Characteristics

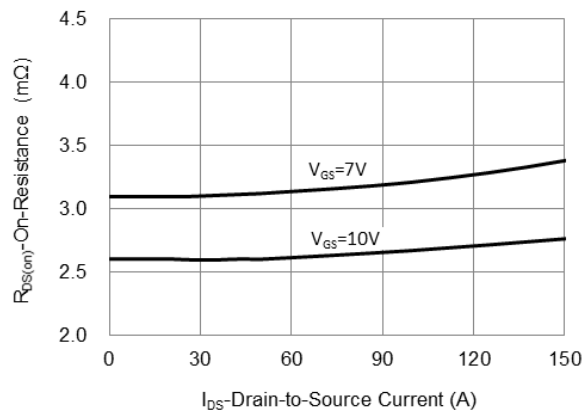


Fig.3 On-Resistance vs. Drain Current

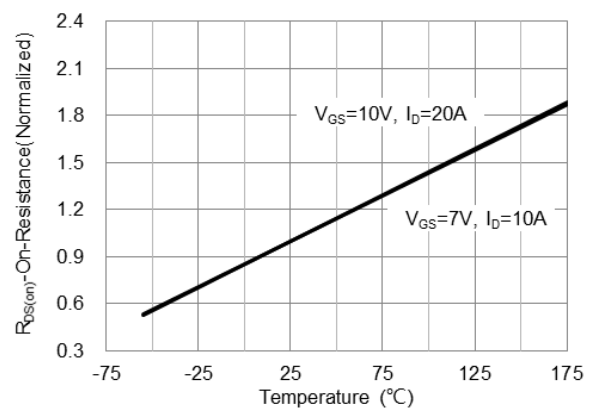


Fig.4 On-Resistance vs. Junction temperature

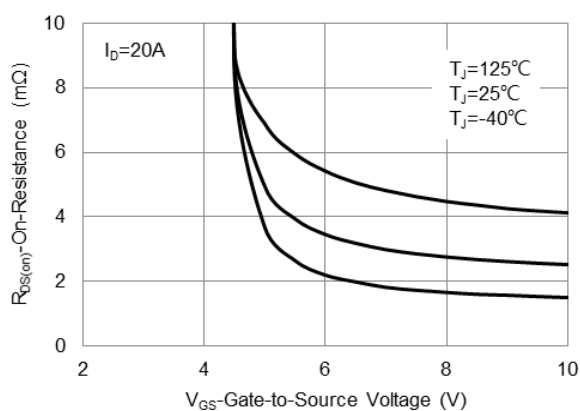


Fig.5 On-Resistance Variation with  $V_{GS}$

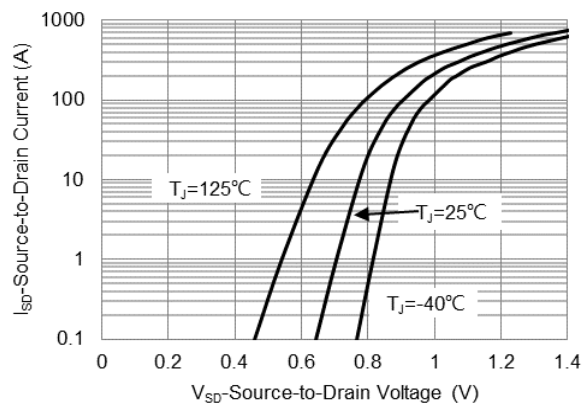


Fig.6 Source-Drain Diode Forward Voltage

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## TYPICAL CHARACTERISTIC CURVES

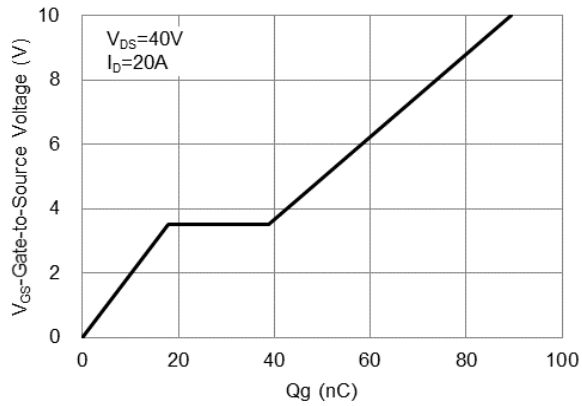


Fig.7 Gate-Charge Characteristics

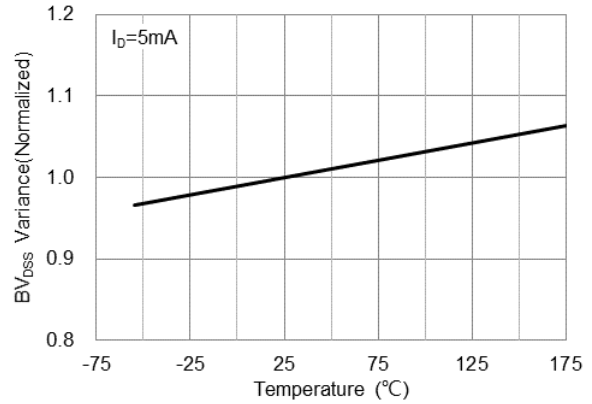


Fig.8 Breakdown Voltage Variation vs. Temperature

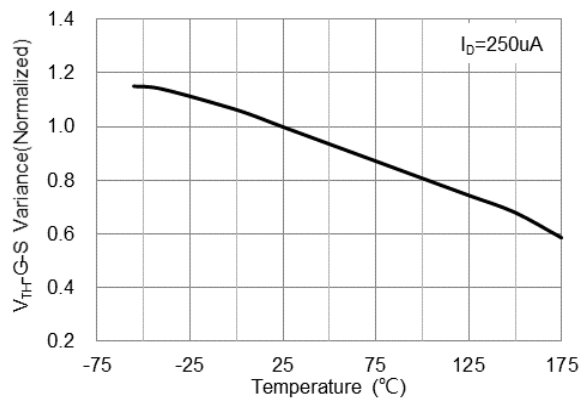


Fig.9 Threshold Voltage Variation with Temperature

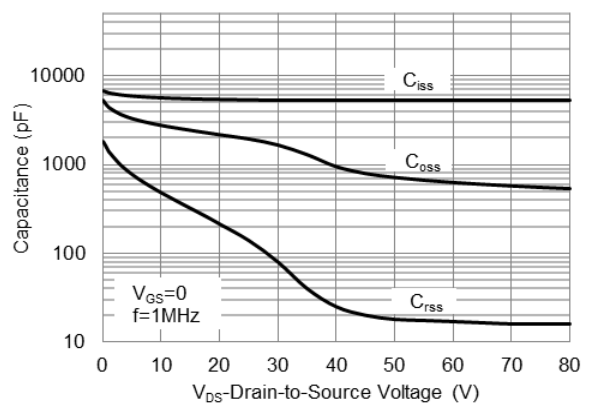


Fig.10 Capacitance vs. Drain-Source Voltage

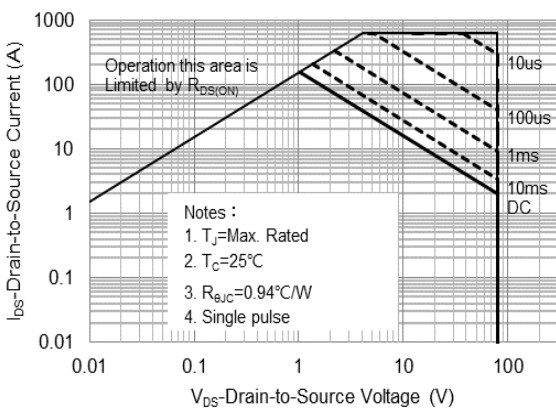


Fig.11 Maximum Safe Operating Area

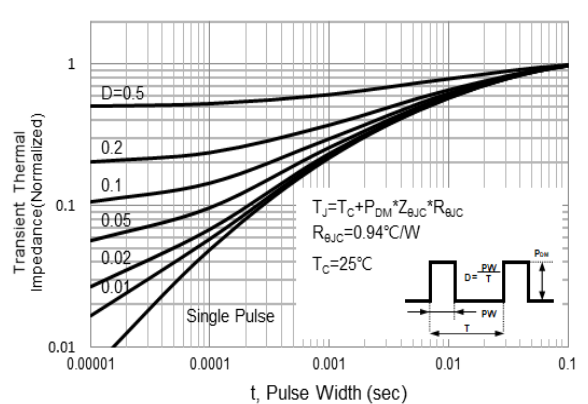


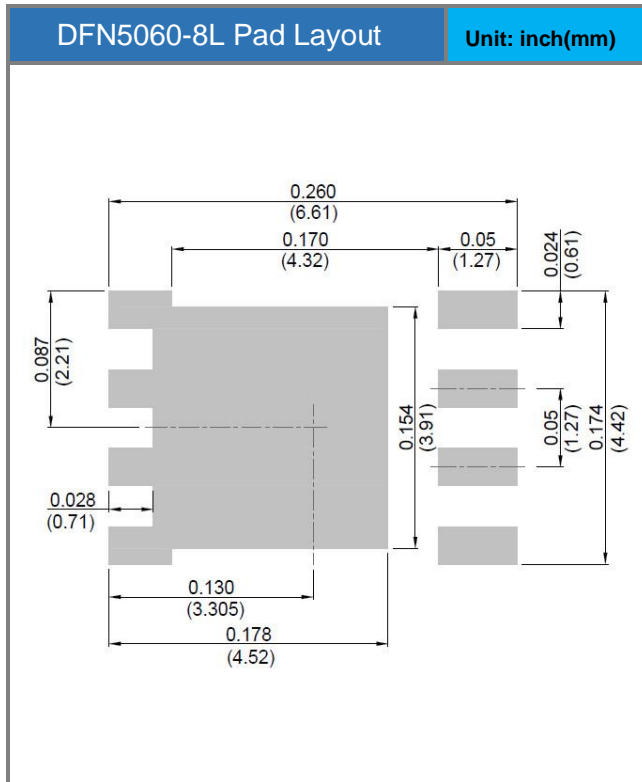
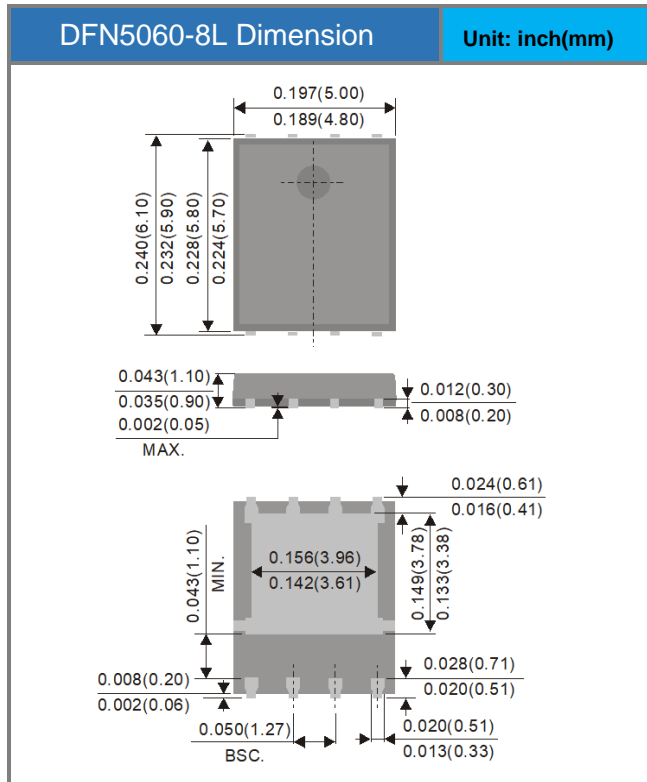
Fig.12 Normalized Transient Thermal Impedance

# PJQ55802-AU

## Product and Packing Information

| Part No.    | Package Type | Packing Type      | Marking |
|-------------|--------------|-------------------|---------|
| PJQ55802-AU | DFN5060-8L   | 3K pcs / 13" reel | Q55802  |

## Packaging Information & Mounting Pad Layout



## PJQ55802-AU

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