

PS2112-D33

Low Capacitance ESD Protection

Voltage

1.5V

Features

- IEC61000-4-2(ESD): $\pm 13\text{kV}$ Air, $\pm 11\text{kV}$ Contact
- IEC61000-4-4(EFT): 40A(5/50ns)
- IEC61000-4-5(Lightning): 4A (8/20 μs)
- Low leakage current, maximum of 0.5 μA at rated voltage
- Low clamping voltage
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard
- Pb-Free/Halogen Free/BFR Free and RoHS Compliant

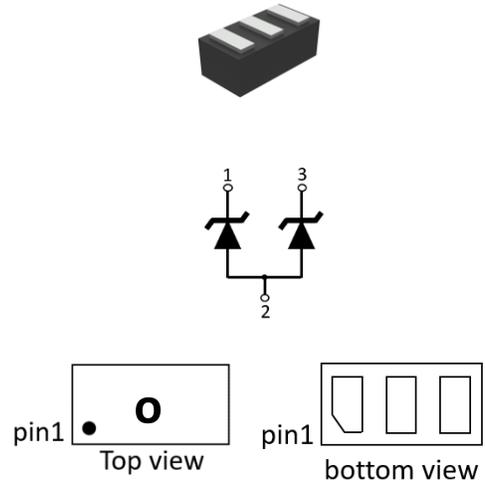
Mechanical Data

- Case: DFN0603-3L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0004 grams

Applications

- Thunderbolt
- USB 3.0/3.1/3.2 and 4.0
- USB Type-C
- Consumer electronics

DFN0603-3L



Part Marking	Parameter
o	o = Marking Code

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
ESD IEC61000-4-2(Air)	V _{ESD}	± 13	kV
ESD IEC61000-4-2(Contact)		± 11	
Operating Junction Temperature Range	T _J	-55~125	°C
Storage Temperature Range	T _{STG}	-55~150	°C

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Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage (Note 2)	V_{RWM}	Pin1/Pin3 to Pin2	-	-	1.5	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1\text{mA}$, Pin1/Pin3 to Pin2	5	-	10	V
Reverse Leakage Current	I_R	$V_{RWM} = 1.5\text{V}$, Pin1/Pin3 to Pin2	-	-	0.5	μA
Surge Clamping Voltage (8/20 μs)	V_{CL}	$I_{PP} = 4\text{A}$, Pin1/Pin3 to Pin2	-	4.2	5.2	V
Clamping Voltage TLP ($t_{\text{period}} = 100\text{ns}$, $t_r = 1\text{ns}$) (Note 3)	V_C	$I_{TLP} = 16\text{A}$, Pin1/Pin3 to Pin2	-	4.9	-	V
Off State Junction Capacitance (Note 4)	C_J	$V_R = 0\text{V}$, $f = 1\text{MHz}$, Pin1/Pin3 to Pin2	-	0.13	0.18	pF

NOTES:

1. Mounted on a FR4 PCB, Single-sided copper, mini pad.
2. A transient suppressor is selected according to the working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operation voltage level.
3. Testing using Transmission Line Pulse (TLP) conditions: $Z_0 = 50 \Omega$, $t_P = 100 \text{ ns}$.
4. This parameter is guaranteed by design.
5. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid the ESD protection device maintain in snap-back state after exceeding breakdown voltage.

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TYPICAL CHARACTERISTIC CURVES

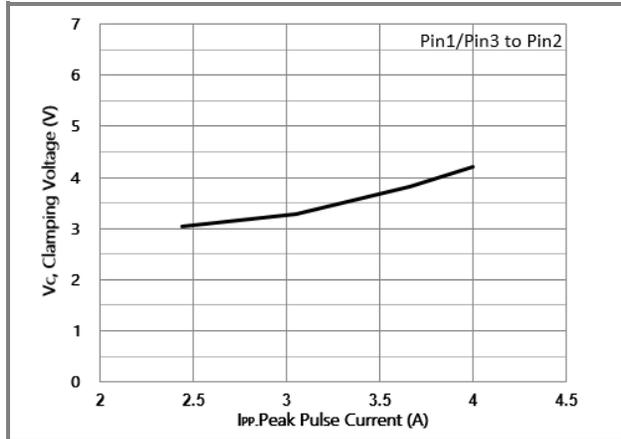


Fig.1 Typical Peak Clamping Voltage

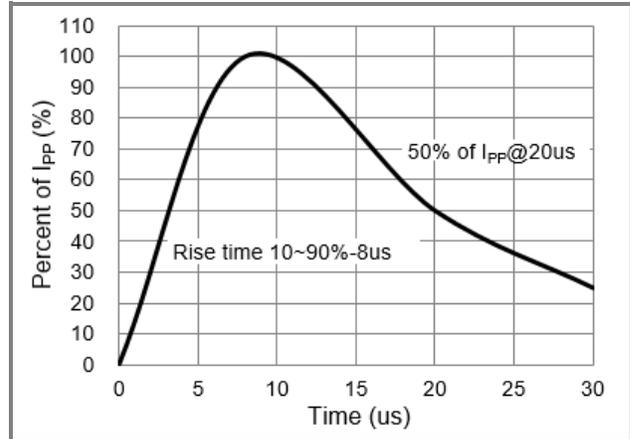


Fig.2 Pulse Waveform

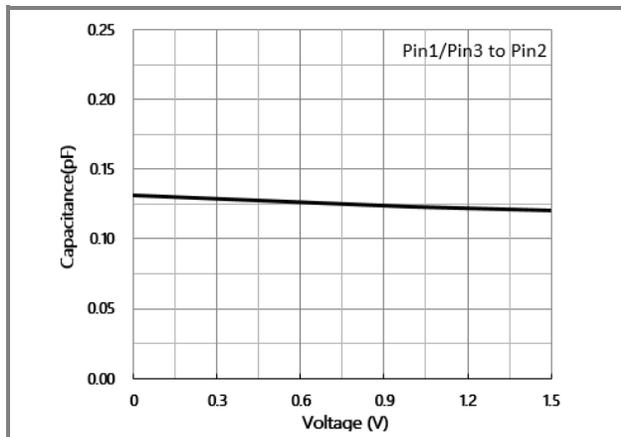


Fig.3 Typical Junction Capacitance

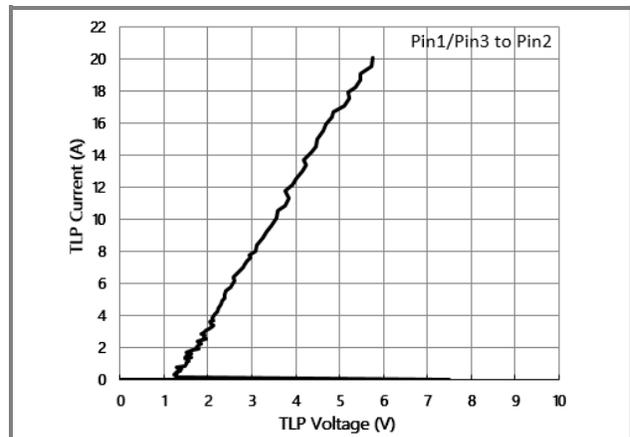


Fig.4 TLP Measurement

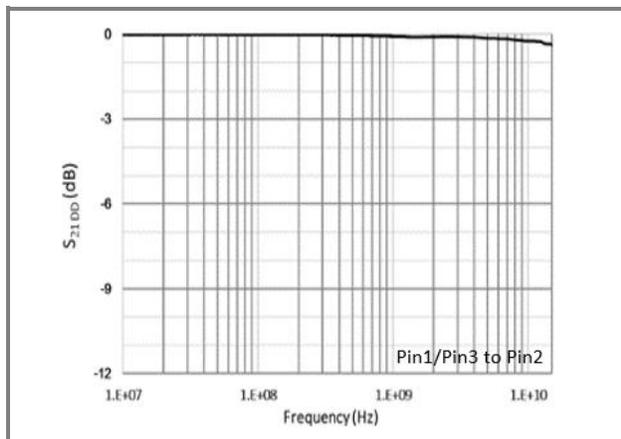


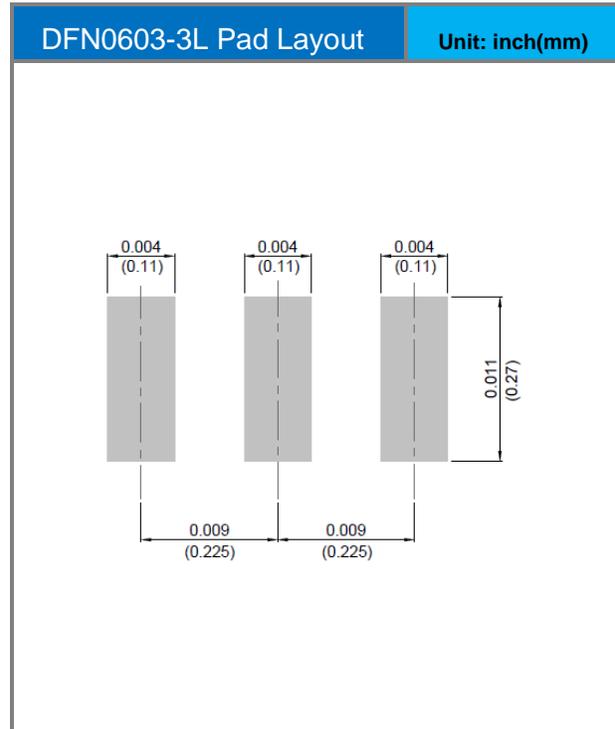
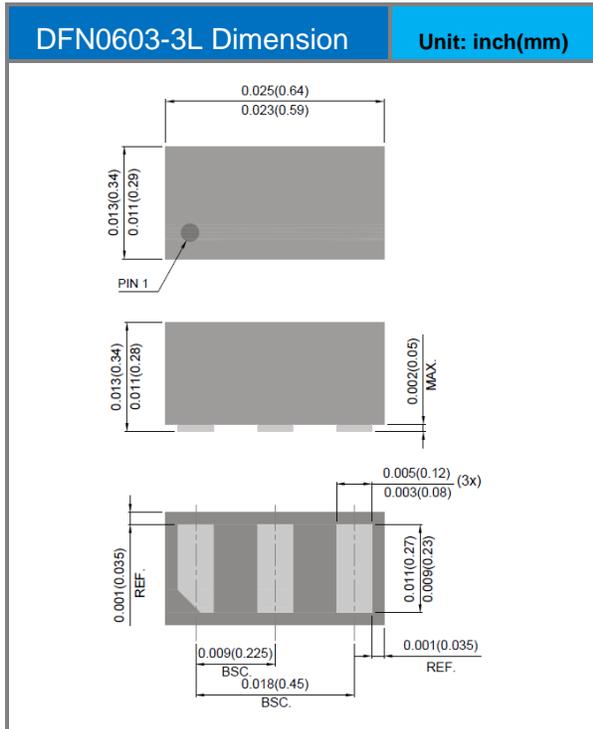
Fig.5 Insertion Loss S₂₁ DD

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Product and Packing Information

Part No	Package Type	Packing Type	Marking
PS2112-D33	DFN0603-3L	10K pcs / 7" Reel	o

Packaging Information & Mounting Pad Layout



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