PJ11036/F

18V, 3A, 600KHz High Efficiency Synchronous, Buck Converter In a SOT23-6 Package

GENERAL DESCRIPTION

PJ11036 is a simple and efficient integrated synchronous buck converter. It features a wide input voltage range of 4.5V to 18V. It supports a continuous output current of up to 3A, with an output voltage range from 0.6V to 7V.

PJ11036 works in pulse frequency modulation (PFM) mode to maintain high efficiency under light loads; PJ11036F operates in forced pulse-width modulation (FPWM) mode to achieve a fixed switching frequency and low output ripple under full load current.

PJ11036 integrated comprehensive protection features, including input under-voltage protection (UVLO), per-cycle valley current limit protection (OCL), output under-voltage protection (UVP), output overvoltage protection (OVP), and over-temperature protection (OTP), to ensure its safe and reliable operation under various working conditions.

PJ11036 assemble in a compact SOT23-6 package and operates within a temperature range of -40°C to 125°C.

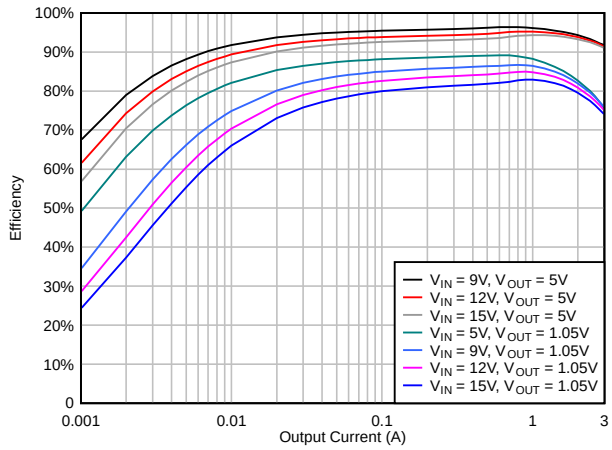
FEATURES

- Wide Operating Input Range : 4.5V to 18V
- Output Voltage Range : 0.6V to 7V
- Continuous Output Current : 3A
- Constant Switching Frequency : 600kHz
- Integrated 90mΩ / 60mΩ Low $R_{DS(ON)}$ MOSFETs
- Low quiescent current (IQ)：190uA (Typ.)
- Low shutdown current (ISD)：2.5uA
- Fast load transient response with COT Control
- Optional Operation Modes Condition :
  - PJ11036 : Pulse Frequency Modulation (PFM)
  - PJ11036F : Forced Pulse Width Modulation (FPWM)
- High Reference Voltage Accuracy : 0.6V ±1.5%
- Complete Protections Integrated for Reliability:
  - Internal 0.8ms Soft-Start Avoiding Inrush Current
  - Cycle-by-Cycle Over Current Limit (OCL) : Peak Current Limit and Valley Current Limit
  - Unlatched VIN UVLO, UVP, OVP and OTP Protection
- Small Solution Size:
  - SOT23-6 Package

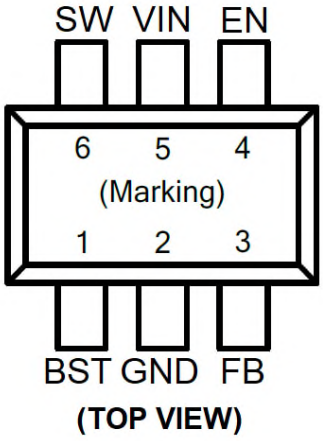
APPLICATIONS

- Digital Set-Top Box and Surveillance
- LCD TV / Monitor
- EPOS
- Home Networking Device and Wireless Router
- Smart Speaker

TYPICAL EFFICIENCY CURVE



PIN CONFIGURATION



ORDERING INFORMATION

ORDER NUMBER	MODE	Marking ID	Package	Description
PJ11036S6_R1	PFM	A2 DNN	SOT23-6	Halogen Free in T&R, 3000 pcs/Reel
PJ11036FS6_R1	FPWM	A7 DNN	SOT23-6	Halogen Free in T&R, 3000 pcs/Reel

FUNCTIONAL PIN DESCRIPTION

TERMINAL		I/O(1)	DESCRIPTION
NUMBER	NAME		
1	BST	P	**Boot-strap Supply Voltage for Internal High-side Driver.** Connect a high-quality 100-nF capacitor from this pin to the SW pin
2	GND	G	**Power Ground and Signal Ground.**
3	FB	I	**Feedback Input**. Sense output voltage through the resistor divider for setting and controlling the output voltage.
4	EN	I	**Enable Control Pin**. Pull high or keep floating to enable the device. Add a pull-up 100kΩ resistor if connect EN to VIN pin. Recommend to add a voltage divider to the EN pin to adjust the VIN start voltage and turn off voltage by custom for reliable turn-on and off.
5	VIN	P	**Input Power Supply.** Add a 100nF ceramic decoupling capacitor as close to VIN and GND pins as possible.
6	SW	P	**Switch Node.** Connect to power inductor with short and wide trace.

(1) I – Input; O – Output; P – Power; G – Ground

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN, SW	-0.3	19	V
	SW, Transient <10 ns	-3	21	V
	VIN – SW	-0.3	19	V
	VIN – SW, Transient < 10 ns	-3	21	V
	BST	-0.3	25	V
	BST – SW	-0.3	6	V
	EN, FB	-0.3	6	V
T_J(2)	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under ***absolute maximum ratings*** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ***recommended operating conditions*** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

HANDLING RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	4.5		18	V
V_{OUT}	Output voltage range	0.6		7	V
F_{SW}	Buck switching frequency range		600		kHz
I_{OUT}	Output DC current range	0		3	A
T_J	Operating junction temperature	-40		125	°C

THERMAL INFORMATION

THERMAL RESISTANCE		SOT23-6	UNIT
Θ_{JA}(2)	Junction to ambient thermal resistance (JESD 51-7)	130.6	°C/W
Θ_{JB}	Junction to PCB thermal resistance	84.6	°C/W
Θ_{JC}	Junction to case thermal resistance	28.4	°C/W
$\Theta_{JA(EVM)}$(1)	Junction to ambient thermal resistance (Specific EVM)	69	°C/W

(1) $R_{\theta JA(EVM)}$ is based on the thermal resistance information measured during the actual operation of the corresponding evaluation Module. EVM information: 60mm x 45mm, FR-4, TG150, 1.6mm thickness, 2-layer 2-Oz Cu copper. Operating Condition: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_A = 25°C. This thermal resistance information is for reference only. The actual thermal resistance depends on PCB board layout, and test environment conditions.

(2) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, V_{IN} = 12V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		18	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising	4.0	4.2	4.4	V
		V_{IN} falling	3.6	3.8	4.0	V
$I_{Q(VIN)}$	Quiescent current into the VIN pin, PJ11036	Non-switching, V_{EN} = 5 V, VFB = V_{REF} x 105%, I_{OUT} = 0 A		190		µA
	Quiescent current into the VIN pin, PJ11036F	Non-switching, V_{EN} = 5 V, V_{FB} = V_{REF} x 105%, I_{OUT} = 0 A		193		µA
$I_{SD(VIN)}$	Shutdown current into the VIN pin	IC disabled, V_{IN} = 12V, V_{EN} = 0V		2.5	4.5	µA
EN						
$V_{EN®}$	EN voltage Rising Threshold	EN Rising, Enable Switching	1.09	1.21	1.27	V
$V_{EN(F)}$	EN voltage Falling Threshold	EN Falling, Disable Switching	1.03	1.13	1.21	V
$I_{EN(P)}$	EN pin Sourcing current	V_{EN} = 1.0V	0.94	1.15	1.6	uA
$I_{EN(H)}$	EN pin Hysteresis current		2.29	2.84	3.82	uA
FB						
V_{FB}	FB Voltage	T_J = 25 °C	0.591	0.6	0.609	V
		T_J = -40 °C to 125 °C, V_{IN} = 12V	0.588	0.6	0.612	V
$I_{FB(LKG)}$	FB Input Leakage Current	T_J = 25 °C	-100	0	100	nA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARUP						
T_{SS}	Internal Fixed Soft-start Time	10% V_{OUT} to 90% V_{OUT}		0.8		mS
T_{DLY}	EN Delay Time	EN High to 1st Switching Pulse		400		uS
SWITCHING FREQUENCY						
F_{SW}	Switching Frequency, CCM Mode	V_{IN} = 12V, V_{OUT} = 1.05V, CCM		600		kHz
POWER STAGE						
$R_{DSON(HS)}$	High-Side MOSFET On-Resistance	T_J = 25 ℃, V_{IN} = 12V, $V_{BOOT-SW}$ = 5V		90		mΩ
$R_{DSON(LS)}$	Low-Side MOSFET On-Resistance	T_J = 25 ℃, V_{IN} = 12V, $V_{BOOT-SW}$ = 5V		60		mΩ
T_{ON_MIN}(1)	Minimum On Pulse Width			50		nS
T_{OFF_MIN}	Minimum Off Pulse Width			200		nS
T_{DEAD}	Dead Time			10		nS
I_{ZC}	Zero-cross detection current			80		mA
OVER CURRENT PROTECTION						
$I_{LS(OC)}$	Low-side Valley Current Limit, PJ11036	V_{IN} = 12V	3.1	3.3	3.5	A
$I_{LS(NOC)}$	Low-side Negative Current Limit, PJ11036F	V_{IN} = 12V	1.15	1.42	1.67	A
OUTPUT OVP AND UVP						
V_{OVP_HYS}	OVP Hysteresis			8		%
V_{OVP_R}	OVP Rising			117		%
V_{UVP_F}	UVP Failing			67		%
V_{UVP_HYS}	UVP Hysteresis			8		%
$T_{HCP(WAIT)}$	Wait Time before Entering UV Hiccup			110		uS
$T_{HCP(OFF)}$	UVP Hiccup Time before Re-startup			12		mS
OVER TEMPERATURE PROTECTION						
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			35		°C

(1) Guaranteed by design

Typical Operating Characteristics

Test Conditions: V_{IN} = 12V, T_A = 25°C (unless otherwise noted)

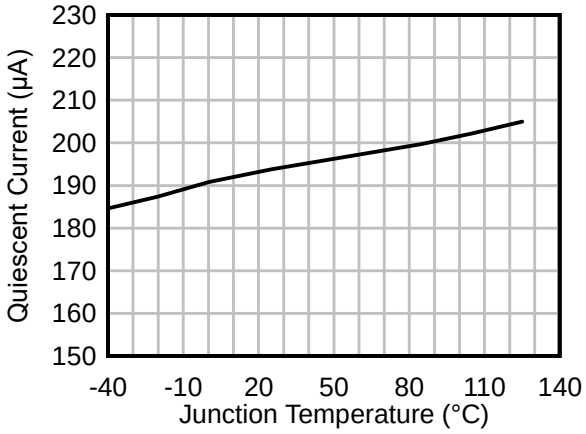


Figure-1. Quiescent Current (PJ11036) VS. Temp.

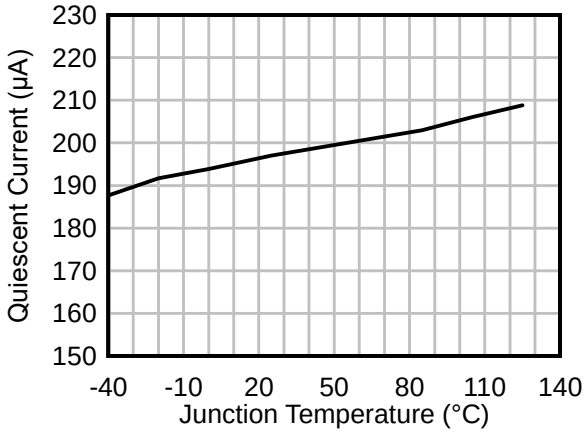


Figure-2. Quiescent Current (PJ11036F) VS. Temp.

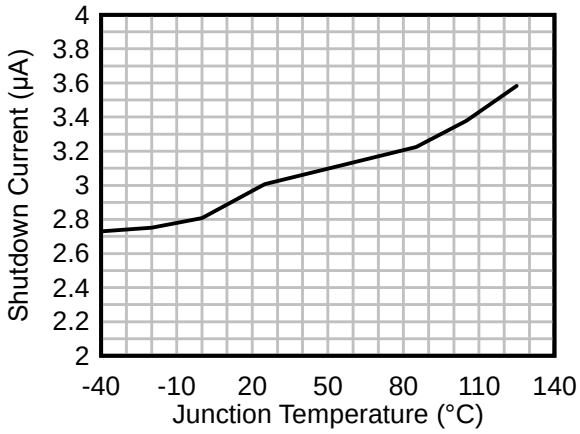


Figure-3. Shutdown Current VS. Temp.

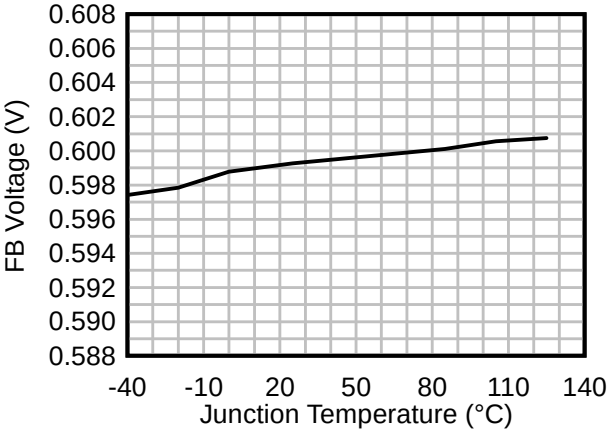


Figure-4. Reference Voltage VS. Temp.

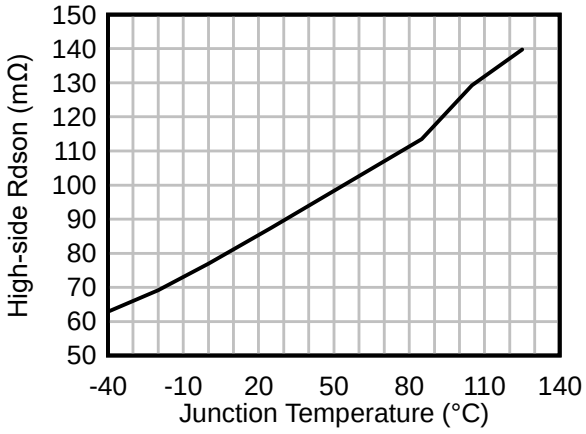


Figure-5. High-Side $R_{DS(ON)}$ VS. Temp.

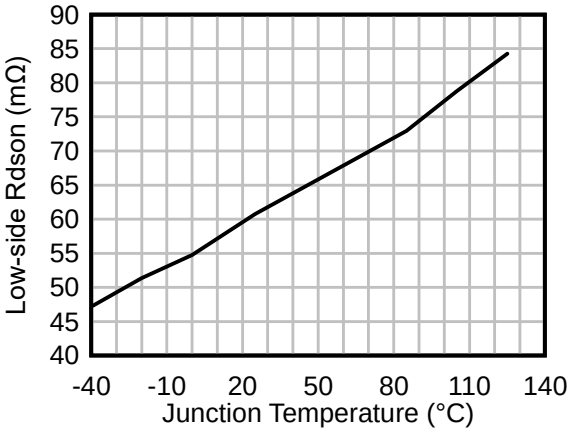


Figure-6. Low-Side $R_{DS(ON)}$ VS. Temp.

Test Conditions: V_{IN} = 12V, T_A = 25°C (unless otherwise noted)

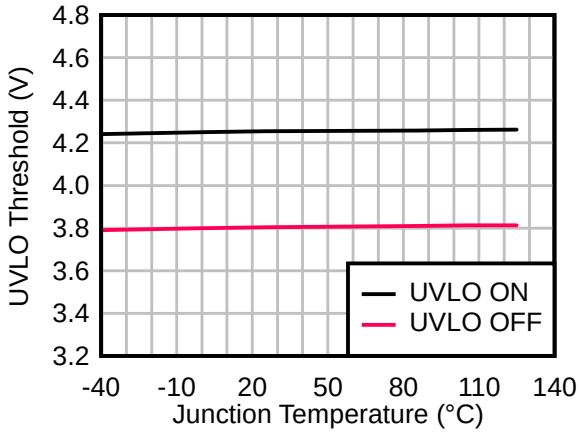


Figure-7. UVLO Threshold VS. Temp.

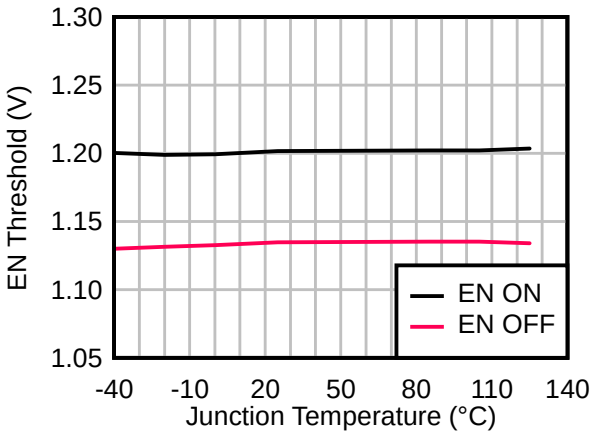


Figure-8. EN Pin Threshold VS. Temp.

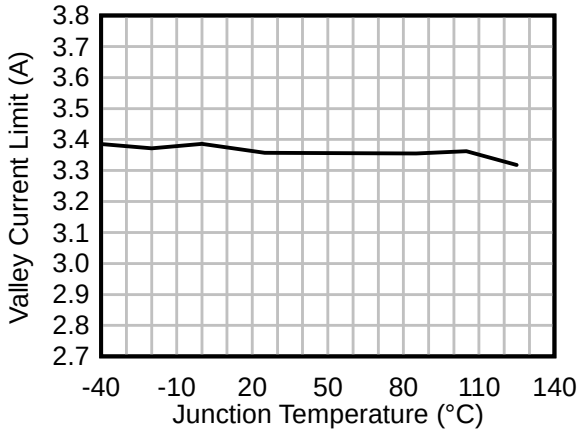


Figure-9. Valley Current Limit VS. Temp.

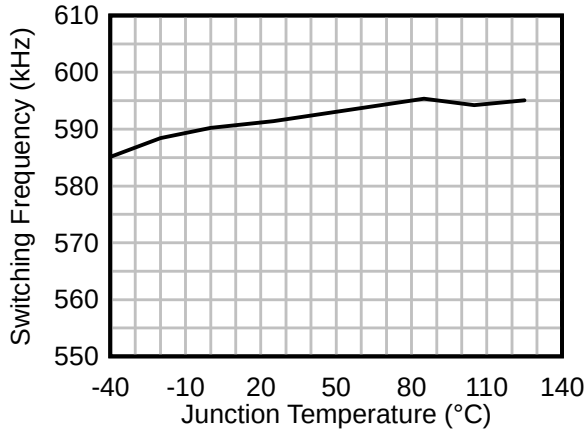


Figure-10. Switching Frequency VS. Temp.

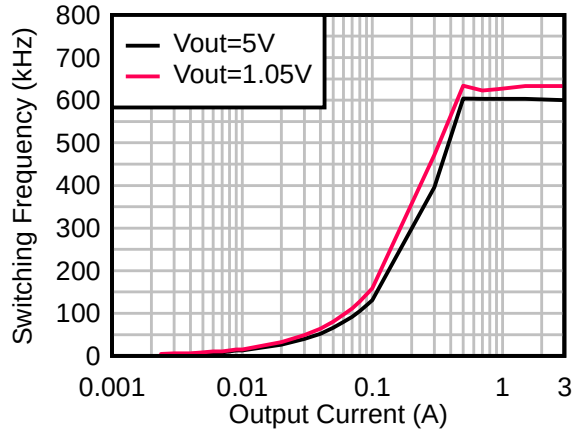


Figure-11. Switching Frequency (PJ11036) VS. I_{OUT}

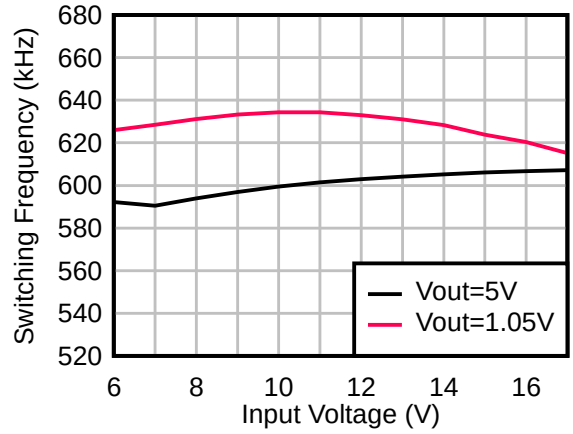
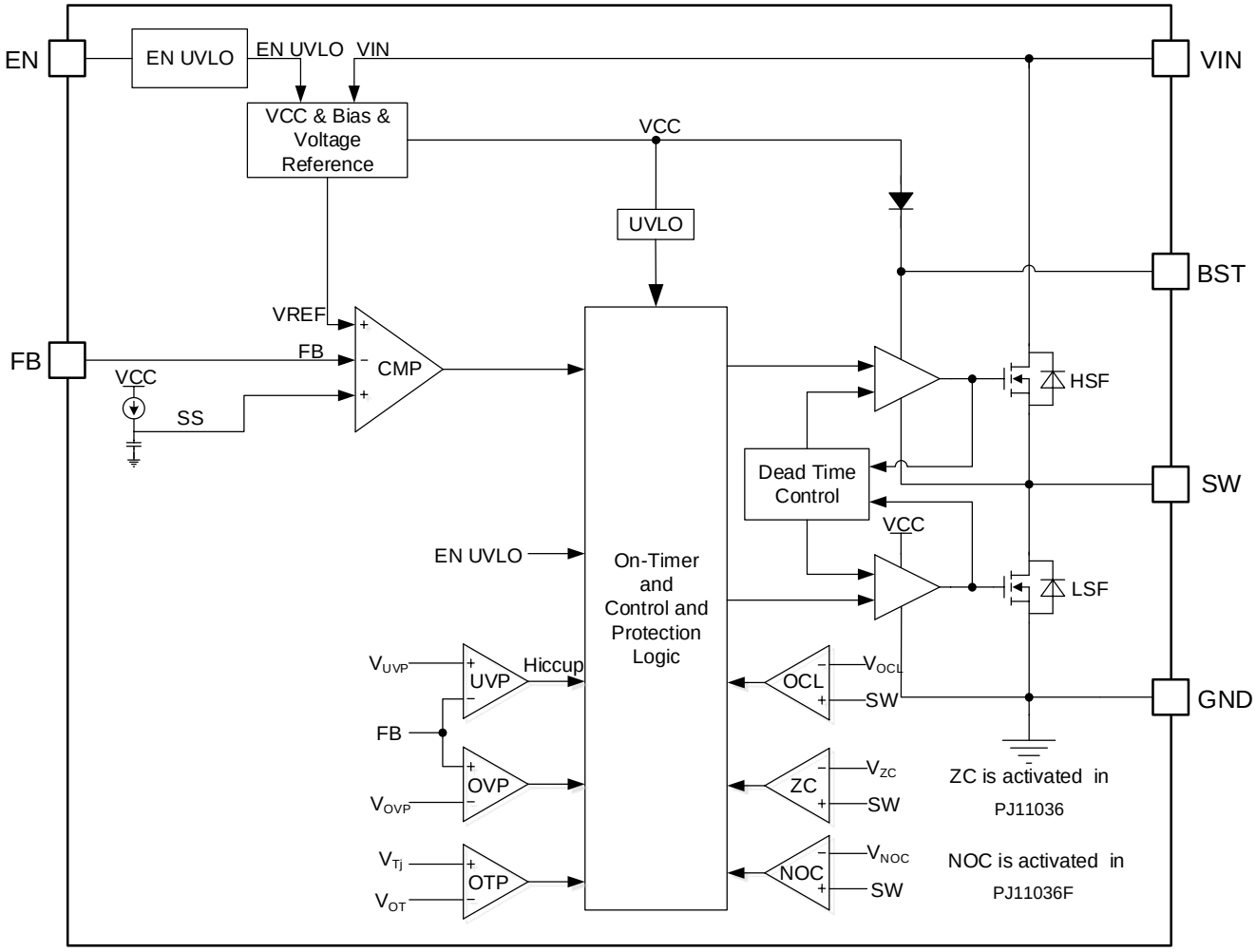


Figure-12. Switching Frequency (PJ11036F) VS. V_{IN}

FUNCTION BLOCK DIAGRAM



FEATURE DESCRIPTION

Overview

PJ11036 is a 3A synchronous buck converter designed for a wide variety of middle voltage applications, especially suited for 12V power rails. The converter adopts constant-on-time (COT) control to provide ultrafast transient response without external loop compensation, helping to save output capacitors and reduce solution size. To achieve pseudo-fixed operation frequency over different conditions, the on-timer is designed inversely proportional to input voltage and directly proportional to output voltage. Also, an error amplifier is integrated to improve the output voltage accuracy and load regulation performance.

At light-load conditions, the PJ11036 operates in power-saving mode (PFM) reducing switching frequency to maintain high light-load efficiency, and PJ11036F operates in forced PWM mode (FPWM) keeping frequency constant to maintain tight output voltage ripples.

Device Operation Modes

Constant On-Time Control

The main control loop of the PJ11036 is constant on-time control (COT) with an error amplifier. The COT control is an output voltage valley-ripple-based control and is based on a comparator and an adaptive one-shot on timer to regulate output voltage.

At the beginning of each cycle, the high-side MOSFET (HSF) is turned on when the FB voltage drops below reference voltage. The HSF is turned on for a fixed interval which is determined by the adaptive one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency nearly constant over input voltage range. Following the on-time, the HSF remains off for a minimum time of 180ns. If FB voltage is below the reference at that time the HSF turns on again for another on-time period. By repeating operation this way, the converter regulates the output voltage with nearly constant frequency.

To achieve stable operation with low-ESR ceramic output capacitors, an internal ripple injection signal is added to the feedback reference voltage to simulate the output voltage ripple. Also, an internal ramp generation signal is integrated to reduce the switching jitters.

Pulse Frequency Modulation and Forced Pulse Width Modulation (FPWM)

PJ11036 automatically enters pulse frequency modulation (PFM) at light-load conditions to maintain high efficiency. As the load current decreases, the inductor current ripple valley eventually touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET (LSF) is turned off when the zero-inductor current is detected. In this case, the output capacitor is only discharged by load current so that the switching frequency decreases. As the result, the light-load efficiency can be enhanced due to lower switching loss.

PJ11036F operates in forced pulse width modulation (FPWM) at light-load conditions to maintain tight output voltage ripples. The LSF is forced on when the HSF is in its off state and after the dead time of 10ns, until the next cycle HSF turns on. This mode allows inductor current flowing from output capacitor to the switching node through LSF's drain-to-source terminals, which is called negative current. In this case, the switching frequency nearly keeps constant over full range of load current achieving tight output voltage ripples.

Precise Enable Control and UVLO

PJ11036 provides an EN pin, as an external IC enable control, to enable or disable the device. When the EN pin voltage rises above the rising threshold voltage ($V_{EN(R)}$) while the V_{IN} voltage is higher than V_{IN} under-voltage lock-out threshold ($V_{UVLO(R)}$), the device turns on. If the EN pin voltage is pulled below the falling threshold voltage ($V_{EN(F)}$), the regulator stops switching and enters the shutdown mode, that is, the regulator is disabled, and switching is inhibited even if the V_{IN} voltage is above V_{IN} under-voltage lock-out threshold ($V_{UVLO(R)}$). During shutdown mode, the supply current can be reduced to $I_{SHDN(VIN)}$ (typical 2.5μA).

The EN pin has an internal pull-up source current, which allows users to float the EN pin to enable the device. If an application requires control of the EN pin, external control logic interface like open drain or open-collector output logic can be connected to the EN pin. EN pin is clamped internally using a 5V series Zener diode (typical break-down voltage is 6.9V). Connecting the EN input through a pull-up resistor (>=100kΩ) to VIN limits the EN input current to prevent damage to the Zener diode.

When connecting the EN pin externally to a voltage higher than 6V, such as VIN voltage, a pull-up resistor (no less than 100kΩ is recommended) should be added in series to limit the input current of the EN pin and prevent damage to the Zener diode, as shown in Figure-13.

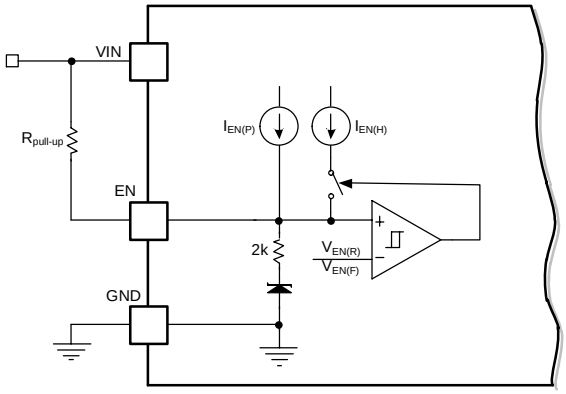


Figure-13. Pull-up Resistor to V_{IN}

The V_{IN} under-voltage lock-out (UVLO) protects the IC from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (V_{CC}). The UVLO rising threshold ($V_{UVLO(R)}$) is about 4.2V, while its falling threshold ($V_{UVLO(F)}$) is 3.8V. If V_{EN} rises above $V_{EN(R)}$ first, switching will still be inhibited until the V_{IN} rises above $V_{UVLO(F)}$. After the device is powered up, if the input voltage V_{IN} goes below $V_{UVLO(F)}$, this switching will be inhibited. If V_{IN} rises above $V_{UVLO(R)}$, the device will resume normal operation with a complete soft-start process again.

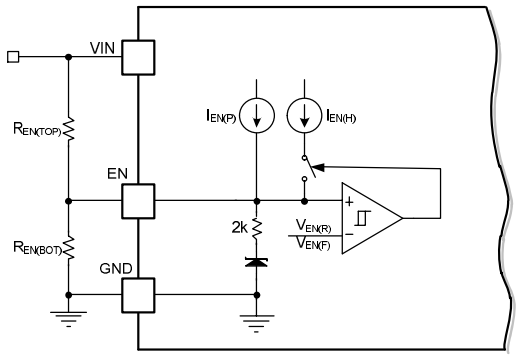


Figure-14. V_{IN} UVLO BLOCK

The rise and fall thresholds of VIN UVLO for PJ11036 are fixed, and the typical hysteresis voltage is 400mV. If a higher threshold and hysteretic voltage need to be set in practical applications, PJ11036 supports custom setting of VIN UVLO threshold by connecting a voltage resistor divider between VIN pin and EN pin, to avoid repeated restart-up of the IC due to VIN spike noise and ringing at the timing of power on and power off, as shown in Figure-14.

The EN pin has a small pull-up current ($I_{EN(P)}$), which sets the default state of the EN pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the external V_{IN} UVLO function because it increases by $I_{EN(H)}$ when the EN pin voltage rises above the EN rising threshold $V_{EN(R)}$. Use Equation-1 and Equation-2 to calculate the values of $R_{EN(TOP)}$ and $R_{EN(BOT)}$ for a specified V_{IN} UVLO threshold, where $V_{IN(START)}$ and $V_{IN(STOP)}$ are the expected input voltage enabling/disabling the IC.

$$R_{EN(TOP)} = \frac{V_{IN(START)} \frac{V_{EN(F)}}{V_{EN(R)}} - V_{IN(STOP)}}{I_{EN(P)}\left(1 - \frac{V_{EN(F)}}{V_{EN(R)}}\right) + I_{EN(H)}}$$

Equation-1

$$R_{EN(BOT)} = \frac{R_{EN(TOP)} V_{EN(F)}}{V_{IN(STOP)} - V_{EN(F)} + R_{EN(TOP)}(I_{EN(P)} + I_{EN(H)})}$$

Equation-2

Soft Start and Pre-biased Soft Start

The PJ11036 provides an internal soft-start feature to ensure inrush control and smooth output voltage ramping during power-up, and the output voltage starts to rise after a 440μs delay from EN rising edge. When the IC starts, the soft-start circuitry generates a soft-start voltage (SS) ramping up from 0V. When it is below the internal reference voltage (V_{REF}), SS overrides V_{REF} so the error amplifier and comparator use SS as the reference voltage. The output voltage smoothly ramps up. Once SS rises above V_{REF}, V_{REF} regains control. At this time the soft start process ends, and the PJ11036 enters steady state operation. The soft start time (T_{SS}) is internal fixed at around 0.8ms (10%V_{OUT} to 90%V_{OUT}).

If the output capacitor is pre-biased at startup, the PJ11036 initiates switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

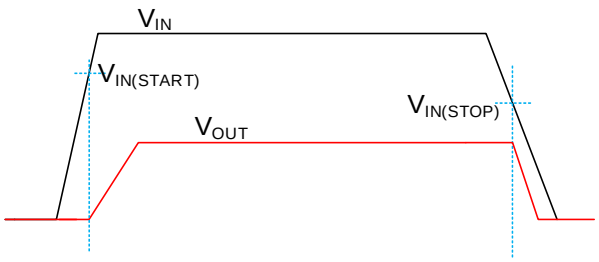


Figure-15. Start-up and Stop Voltage

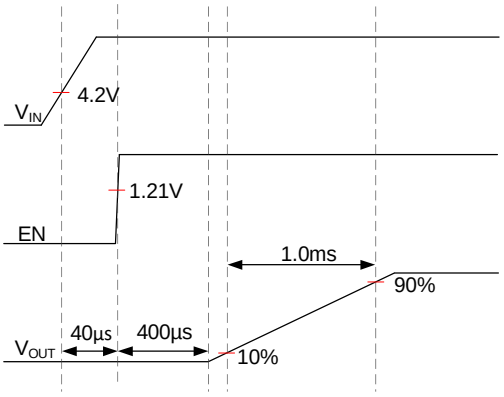


Figure-16. Soft-Start Timing Diagram

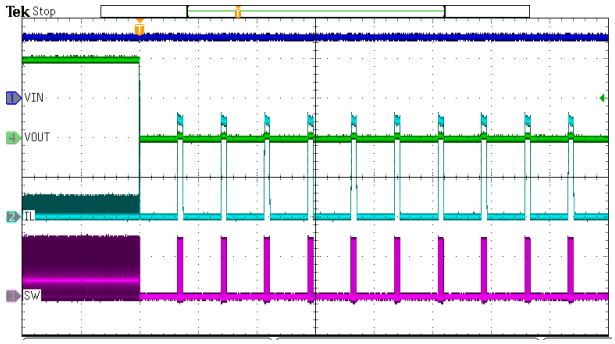


Figure-17. UVP Hiccup mode

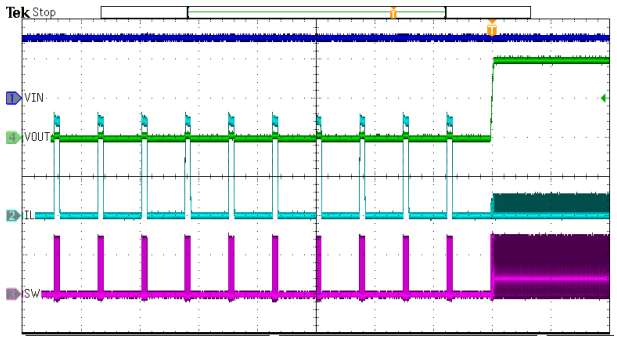


Figure-18. UVP Hiccup recovery

Output UVP with Hiccup mode

PJ11036 integrates output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (V_{UVP}) (typically 65% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

If the output under-voltage condition continues for a period time of $T_{HCP(WAIT)}$, the PJ11036 will enter output under-voltage protection (UVP) with hiccup mode. During hiccup mode, the IC will shut down for a period time of $T_{HICCUP(OFF)}$, and then attempt to recover automatically. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. The hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then the converter resumes normal operation as soon as the over-load or short-circuit condition is removed.

Peak and Valley Over-Current Limit

PJ11036 has a valley over-current limit control (OCL). The inductor current is monitored during the LS-FET on state. When the sensed inductor current reaches the valley current limit ($I_{LS(OC)}$), the LS limit comparator turns over, and the PJ11036 enters OCL mode. The HS-FET waits until the valley current limit is removed before turning on again. If the output load current exceeds the available inductor current (clamped by OCL), the output capacitor needs to supply the extra current so that the output voltage will begin to drop. If it drops below the output under-voltage protection threshold (VUVP), the IC will stop switching into UV hiccup mode to avoid excessive heat.

Negative Over-Current Limit (PJ11036F only)

PJ11036F is the part which is FPWM part and allows negative current operation. In case of FPWM operation, high negative current may be generated as an external power source is tied to output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current in each on-time interval of low-side MOSFET and compares

it with negative over-current limit threshold (I_{NOC}). Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy of output inductor. This behavior can keep the valley of negative current at NOC threshold to protect low-side MOSFET. Note that the NOC limit is not in effect during minimum off-time period.

Output Over-Voltage Protection

PJ11036 integrates output over-voltage protection (OVP) to minimize output voltage overshoot and protect down-stream devices when recovering from output fault conditions or strong unload transients. The OVP circuitry detects overvoltage condition by monitoring the feedback voltage (V_{FB}). When V_{FB} rises above the OVP threshold (V_{OVP}), the OVP comparator output turns high and both HSF and LSF turns off to avoid V_{OUT} further rising higher. Once the V_{OUT} drops below V_{OVP} falling threshold, the IC starts switching again. This function is a non-latch operation.

Over Temperature Protection

PJ11036 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold ($T_{J(SD)}$). Once the junction temperature cools down by a thermal shutdown hysteresis ($T_{J(HYS)}$), the IC will resume normal operation with a complete soft start.

APPLICATION INFORMATION

Overview

The output stage of synchronous step-down converter is mainly composed of inductor and capacitors. By switching the internally integrated power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained. This section describes the detailed design process based on one design example.

Output Voltage Setting

As shown in Figure-19, PJ11036 can be set to different output voltages by using an external voltage resistor divider connected to the FB pin. The formula for the output voltage versus the external divider resistor is as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB(T)}}{R_{FB(B)}}\right) \qquad \textbf{Equation-3}$$

Where V_{REF} = 0.6V

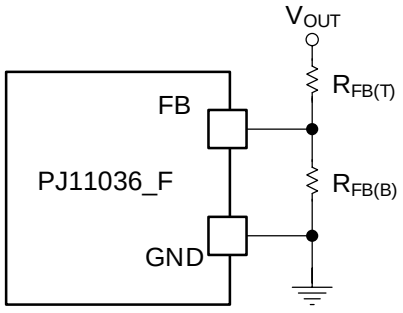


Figure-19. Output voltage setting

It is recommended to design from the bottom side feedback resistor $R_{FB(B)}$. Too large $R_{FB(B)}$ will make the FB pin more susceptible to external noises, while too small $R_{FB(B)}$ will increase the power loss of the resistor divider. $R_{FB(B)}$ = 10kΩ~50kΩ is recommended. And the top side feedback resistor $R_{FB(T)}$ can be calculated by the following formula:

$$R_{FB(T)} = R_{FB(B)} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \qquad \textbf{Equation-4}$$

Where V_{REF} = 0.6V

For example, in the application with 5V output voltage, First, chose $R_{FB(B)}$ as 10kΩ and then $R_{FB(T)}$ is calculated as 73.3kΩ, so the nearest nominal resistor of 73.2kΩ is chosen.

In the application scenarios where higher precision of output voltage is required, it is recommended to select a voltage resistor divider with a precision of 1% or even higher.

PJ11036 is designed to operate in the 4.5V to 18V range. The BUCK converter requires the input voltage to be higher than the output voltage for proper operation. The maximum duty cycle is 75%, so the minimum input voltage is V_{OUT}/0.75. The chip does not allow the output voltage to be higher than the input voltage. Under such conditions, the output capacitors discharges through the body diode of the high-side power MOSFET. The resulting current can cause unpredictable behavior, and in extreme cases, possible device damage. If the application allows for this possibility, then use a Schottky diode from VIN to VOUT to provide a path around the regulator for this current.

Input Startup and Shutdown Voltage Setting

As shown in Figure-15. VIN UVLO Threshold Setting and Figure-16. Input Startup Voltage and Shutdown Voltage Schematic, set the input startup voltage, $V_{IN(START)}$, and the input shutdown voltage, $V_{IN(STOP)}$, respectively, by configuring the EN divider resistor.

In this example, if the input voltage is 12V and the output voltage is 5V, you can select an EN resistor to set the input start voltage $V_{IN(START)}$ to 8V and input shutdown voltage $V_{IN(STOP)}$ to 7V.

According to “Electrical Characteristics”, $V_{EN(R)}$ = 1.21V, $V_{EN(F)}$ = 1.13V, $I_{EN(P)}$ = 1.15μA, $I_{EN(H)}$ = 2.84μA were substituted into Equation-1 and Equation-2

to get $R_{EN(TOP)}$ = 162kΩ, $R_{EN(BOT)}$ = 28kΩ.

In addition, for applications where the EN pin is directly controlled by digital signals such as GPIO port, it can be directly connected to the EN pin by GPIO port. If need to disable IC when the GPIO port is in a high resistance state, it is recommended to add a pull-down resistor of less than 500 kΩ to the EN pin.

Output Inductor Selection

The selection of inductor is related to the size, cost, efficiency, and transient response performance. Three key parameters of inductor are mainly considered: inductance (L), saturation current (I_{SAT}) and inductor DC resistance (DCR).

To compromise the volume and power consumption of the inductor, it is recommended to select an inductor whose current ripple (ΔI_L) is 20%-50% of the rated current (I_{rated}) of PJ11036, as shown in the following formula:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{rated} \times K_L}$$

Equation-5

where

V_{IN} is input voltage,

V_{OUT} is output voltage,

f_{SW} is switching frequency,

I_{rated} is the rated current of 3A

K_L is the current ripple factor : 20%-50%

PJ11036 adopts COT control architecture and has been optimized for common output voltage rails. It is recommended to directly select inductor according to Table-1. Once the inductor has been selected, the actual inductor current ripple ΔI_L and peak current ($I_{L(peak)}$) can be calculated by the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

Equation-6

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Equation-7

where

$I_{OUT(MAX)}$ is the maximum output current

The inductor whose saturation current I_{SAT} is at least greater than the peak current $I_{L(peak)}$ should be selected with a some margin (for example, 10%) to ensure that the inductor will not be saturated during normal steady-state operation of the chip.

Since the inductor current may temporarily rise to greater than the peak current $I_{L(PEAK)}$ of steady-state operation under the conditions of power-up, output overcurrent or load transient of the chip, the more conservative choice is to select the inductor whose saturation current I_{SAT} is greater than the chip current limit $I_{L(MAX\_PEAK)}$, so as to ensure that the inductor will not be saturated under all conditions, as shown in the following formula:

$$I_{L(max\_peak)} = I_{LS(OC)} + \Delta I_L$$

Equation-8

where

$I_{LS(OC)}$ is the valley current value of the chip

$I_{L(MAX\_PEAK)}$ is the max peak inductor current at overcurrent conditions

Considering that the output voltage of this example is 5V, the nominal inductor of 4.7μH can be directly selected according to Table-1. Then the actual inductor ripple and peak current are:

$$\Delta I_L = \frac{5 \times (12 - 5)}{12 \times 580k \times 4.7\mu} = 1.07A$$

$$I_{L(peak)} = 3 + \frac{1.07}{2} = 3.535A$$

When selecting an inductor of 4.7μH, ensure that the saturation current and rated current are at least 3.535A. In addition, the peak inductor current considering overcurrent condition can be calculated as:

$$I_{L(max\_peak)} = 3.3 + 1.07 = 4.37A$$

So the most conservative option is to ensure that the saturation current of the selected inductor is greater than 4.37A.

Output Capacitor Selection

The selection of output capacitor is related to the output voltage ripple and load transient performance. PJ11036 adopts COT control architecture supporting the usage of ceramic capacitors to achieve ultra-fast transient performance while maintaining IC's stable operation. To achieve the most appropriate transient response performance, it is recommended to refer to Table-1 for the selection of output capacitor and inductor.

Output voltage ripple V_{RIPPLE} consists of two main parts. One is the resistive ripple $V_{RIPPLE(ESR)}$ generated by the inductive current at the equivalent series resistance ESR of the output capacitor. The other part is capacitive ripple $V_{RIPPLE(C)}$ generated by charging and discharging the output capacitor with the inductance ripple current. The calculation formula is as follows:

$$V_{RIPPLE} = \sqrt{V_{RIPPLE(ESR)}^{2} + V_{RIPPLE(C)}^{2}} \quad \textbf{Equation-9}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times ESR \quad \textbf{Equation-10}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{sw}} \quad \textbf{Equation-11}$$

The actual ripple can simply be estimated as:

$$V_{RIPPLE} > Max\left(V_{RIPPLE(ESR)}, V_{RIPPLE(C)}\right)$$
$$V_{RIPPLE} < V_{RIPPLE(ESR)} + V_{RIPPLE(C)} \quad \textbf{Equation-12}$$

Considering this design example, according to Table-1, two ceramic capacitors of 22μF/16V are selected as output capacitors. In the case of DC bias with output voltage V_{OUT} = 5V, the actual total effective capacitance is 14μF (7μFx2), and the actual equivalent ESR is 0.86mΩ (1.6mΩ/2). The output ripple V_{RIPPLE} can be calculated as follows:

$$V_{RIPPLE(ESR)} = 1.07 \times \frac{1.6m}{2} = 0.856mV$$

$$V_{RIPPLE(C)} = \frac{1.07}{8 \times 14\mu \times 580k} = 16.5mV$$

$$V_{RIPPLE} = \sqrt{16.5^2 + 0.856^2} = 16.52mV$$

Input Capacitor Selection

Since the input current of the buck converter is a pulsed discontinuous current, it is recommended to use a ceramic capacitor at the input to provide a pulsed input current thus keeping the DC input voltage stable. The ripple on the input capacitance of a ceramic capacitor can be calculated by the following equation:

$$V_{IN(Ripple)} \approx D \times I_{OUT} \times \frac{1 - D}{C_{IN} \times f_{sw}} + I_{OUT} \times ESR$$

Equation-13

Where $D = \frac{V_{OUT}}{V_{IN}}$

In addition, since the input capacitance is a pulsed discontinuous current, the selected input capacitor must be able to withstand a large AC RMS current:

$$I_{IN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D(1 - D)} \quad \textbf{Equation-14}$$

In order to optimize the EMI performance of the chip and to ensure reliable and stable, it is recommended to add a 0.1μF ceramic capacitor (0603/0402 package) in addition to the ceramic capacitor as input capacitance C_{IN}, and place it as close as possible to the VIN and GND pins of the chip. It should be noted that although ceramic capacitors have excellent high frequency performance and stable lifetime, in some hot-swap scenarios, the actual V_{IN} voltage may oscillate due to the low ESR of the ceramic capacitors, and in the worst case, it may oscillate up to 2 times the V_{IN} voltage, which can cause over-voltage breakdown of the chip. In this case, it is recommended to add an additional electrolytic capacitor with a larger ESR or a TVS diode in parallel with the input voltage to limit the input overvoltage.

Table-1 Recommended Component Selection Table

V_{OUT} (V)	$R_{FB(T)}$ (kΩ)	$R_{FB(B)}$ (kΩ)	L_{min} (μH)	L_{typ} (μH)	L_{max} (μH)	$C_{OUT(EFF)}$ (μF)(1)
5.0	73.2	10	3.3	4.7	5.6	10 to 68
3.3	45.3	10	2.2	3.3	4.7	10 to 68
2.5	31.6	10	2.2	2.2	4.7	20 to 68
1.8	20.0	10	1.5	2.2	4.7	20 to 68
1.5	15.0	10	1.5	1.5	4.7	20 to 68
1.2	10.0	10	1.2	1.5	4.7	20 to 68
1.05	7.5	10	1.0	1.5	4.7	20 to 68
1	6.65	10	1.0	1.2	4.7	20 to 68

(1) $C_{OUT(EFF)}$ is the total effective capacitance. Considering effective capacitance de-rating, which is related to biased voltage level and size, the effective capacitance of C_{OUT} at target output level should meet the value in above table to make converter operated in stable and normal.

Feedforward Capacitor Selection

PJ11036 utilizes the COT control architecture to achieve ultra-fast load transient response performance. In some applications where the load transient response is more demanding, the transient response can be further improved by adding a R_{FF}, and a C_{FF}, to the output feedback divider resistor. Considering the influence of noise coupling, it is recommended to use R_{FF} = 2 kΩ~10 kΩ, and do not use C_{FF} higher than 100 pF. Note that the actual R_{FF} and C_{FF} are optional devices, and it is recommended to optimize the selection based on the results of the measured load transient response and the output tuning rate.

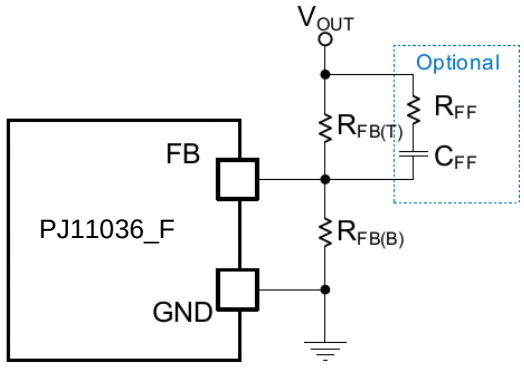


Figure-20. Feedforward Resistor and Capacitor

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between the BST to SW pin for proper operation. At least 10V X5R or X7R 0.1μF ceramic capacitor of 0603 package is recommended.

PCB Design Guidelines

PCB design is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Position the input ceramic capacitors as close to the VIN and GND pins as possible.

2. Keep the alignment of the power circuit (CIN→L →COUT→GND) as short and wide as possible to minimizes circuit voltage drop and enhances conversion efficiency.

3. The voltage waveform of the SW node forms a high-frequency square wave. Appropriately reducing the copper spreading of the SW node can enhance EMI performance. Conversely, increasing the spreading can optimize heat dissipation. The user should make the appropriate decision considering these factors

based on the actual situation.

4. Leave a considerable distance between the FB pin and noise sources like the SW node and BST node.

5. Place the sampling point of the output voltage V_{OUT} close to the end of the output capacitor, and position the voltage divider sampling resistor near the FB pin.

6. Route and spread the copper of VIN and GND as wide as possible to help heat dissipation. In multilayer PCB design, it is recommended to have a complete GND layer for the GND pin and to add enough vias between the GND layer and the chip layer.

PCB design example is shown below:

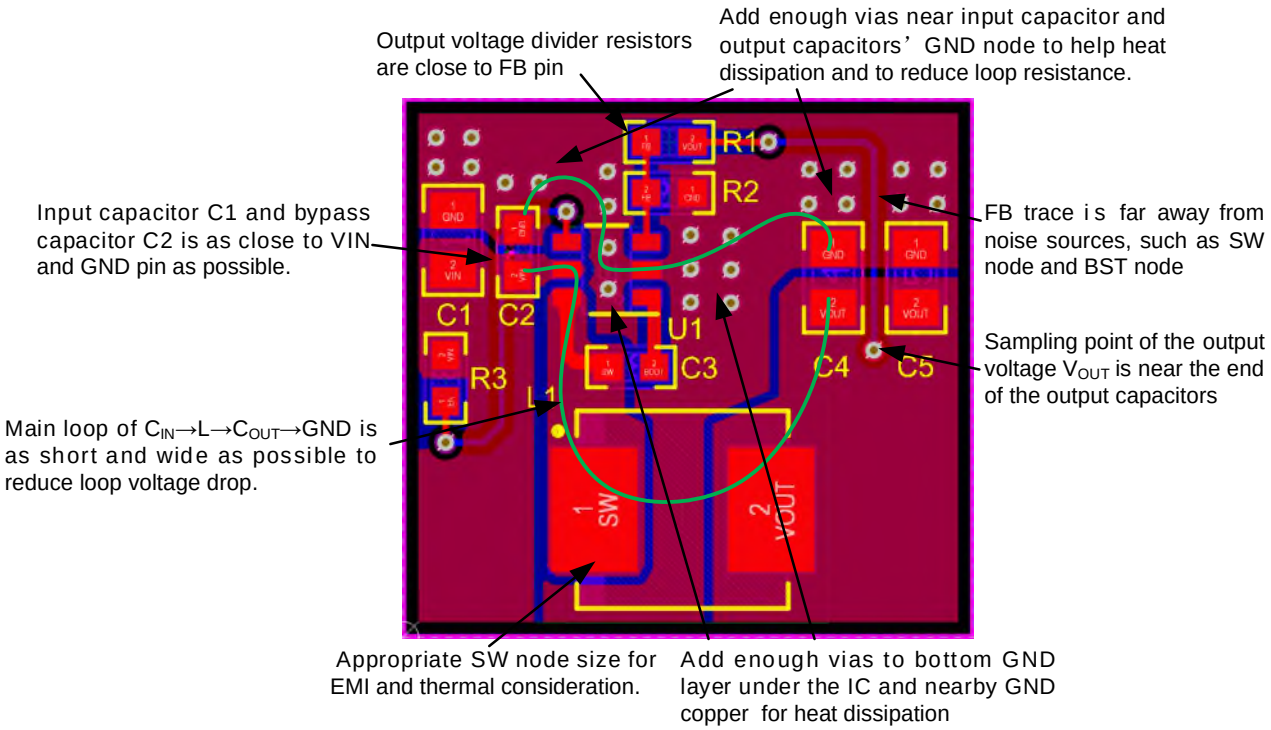


Figure-21. PCB Design Example

Typical Reference Design

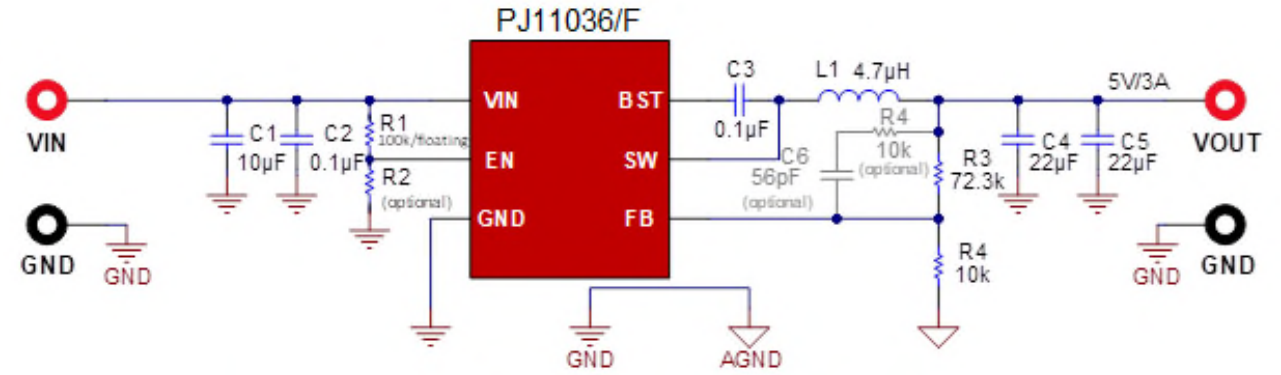


Figure-22. V_{IN}= 12V, V_{OUT}= 5V, I_{OUT}= 3A

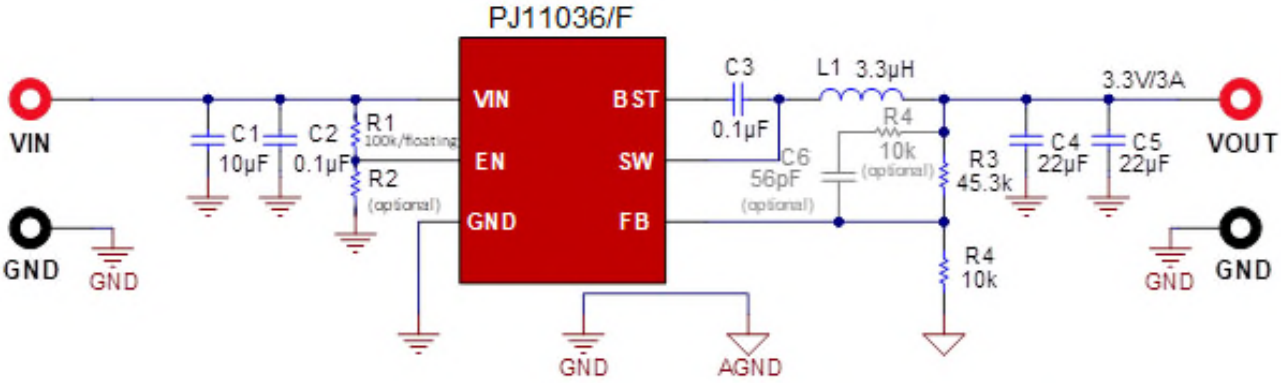


Figure-23. V_{IN}= 12V, V_{OUT}= 3.3V, I_{OUT}= 3A

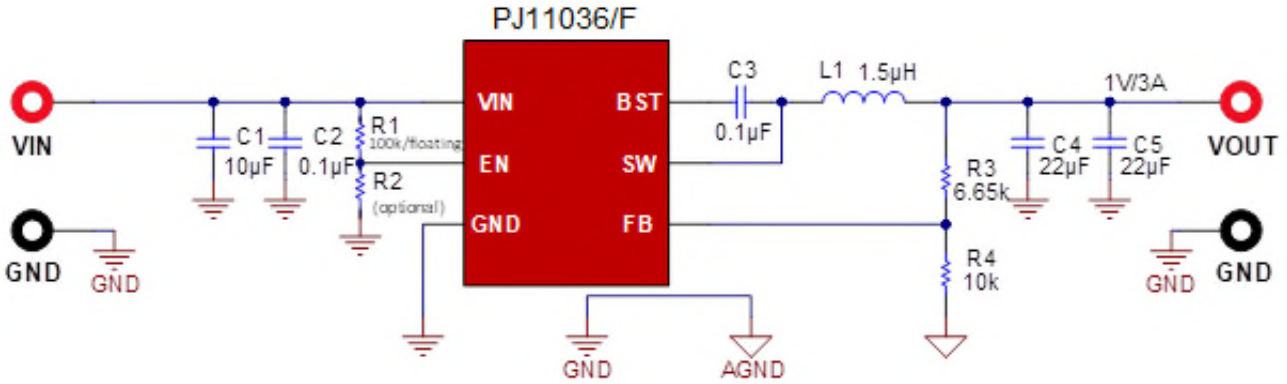


Figure-24. V_{IN}= 12V, V_{OUT}= 1.0V, I_{OUT}= 3A

Typical Operating Characteristics

Test Conditions: V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C (unless otherwise noted)

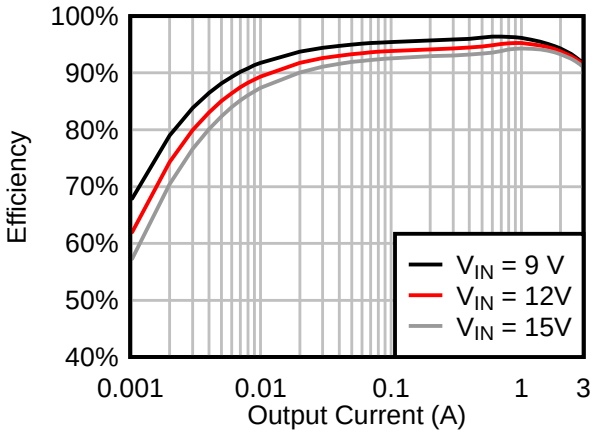


Figure-25. PJ11036 V_{OUT} = 5V Efficiency
L = 4.7μH, DCR = 33mΩ

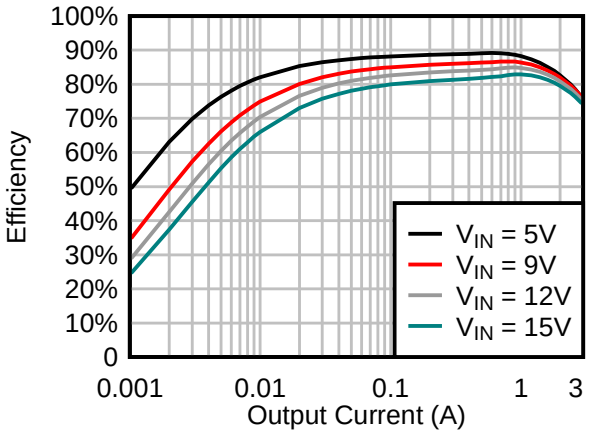


Figure-26. PJ11036 V_{OUT} = 1.05V Efficiency
L = 1.5μH, DCR = 12mΩ

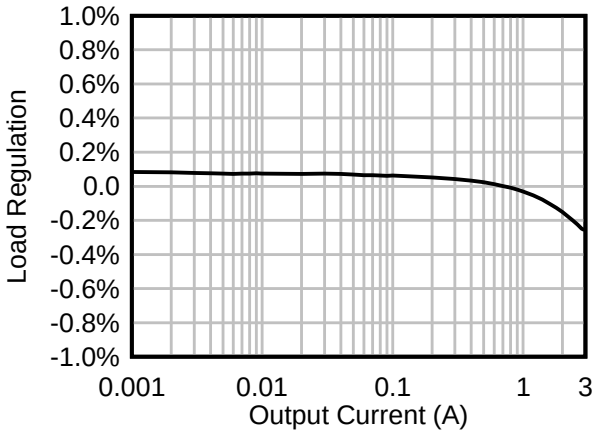


Figure-27. PJ11036 Load Regulation V_{OUT} = 5V

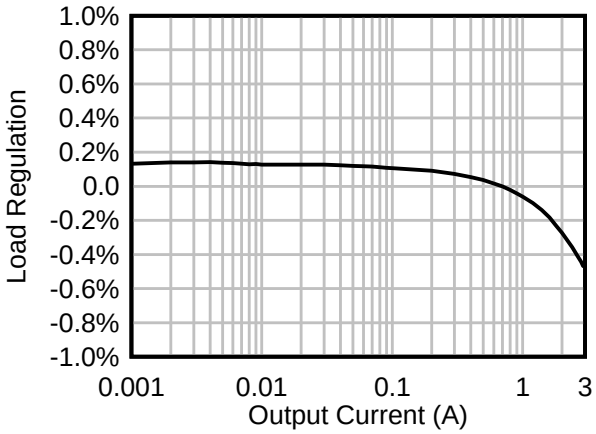


Figure-28. PJ11036 Load Regulation V_{OUT} = 1.05V

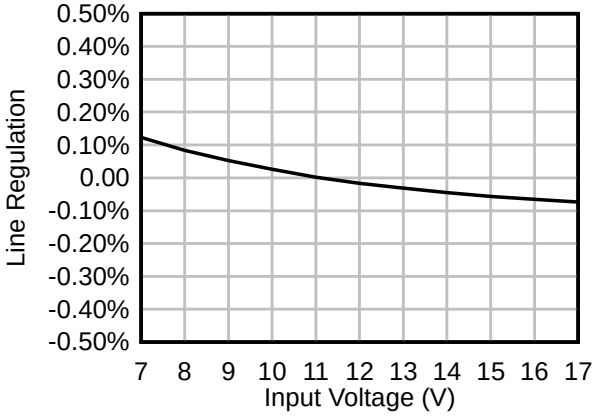


Figure-29. PJ11036 Line Regulation V_{OUT} = 5V

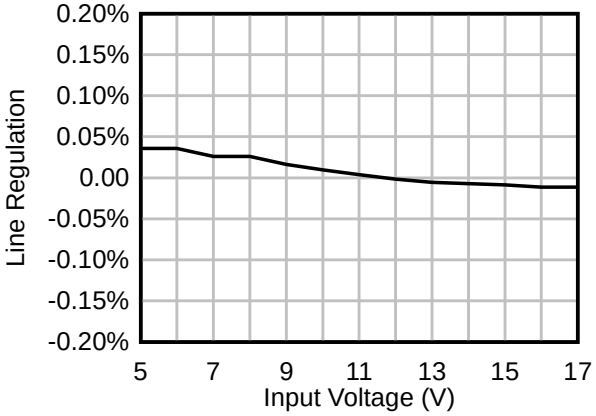


Figure-30. PJ11036 Line Regulation V_{OUT} = 1.05V

Test Conditions: V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C (unless otherwise noted)

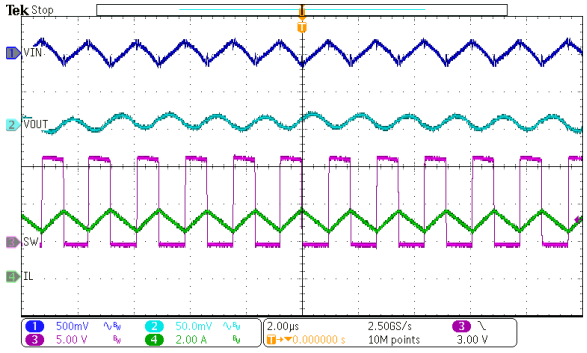


Figure-31. Input Voltage Ripple, I_{OUT} = 3A

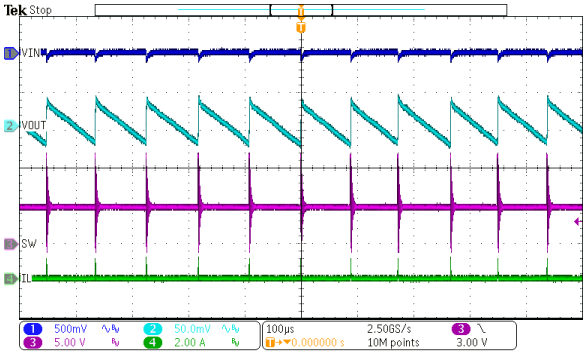


Figure-32. Output Voltage Ripple, I_{OUT} = 10mA

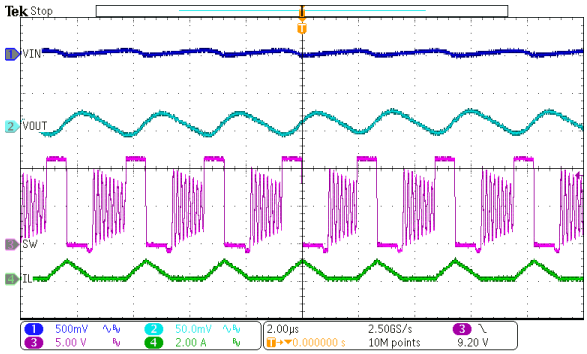


Figure-33. Output Voltage Ripple, I_{OUT} = 250mA

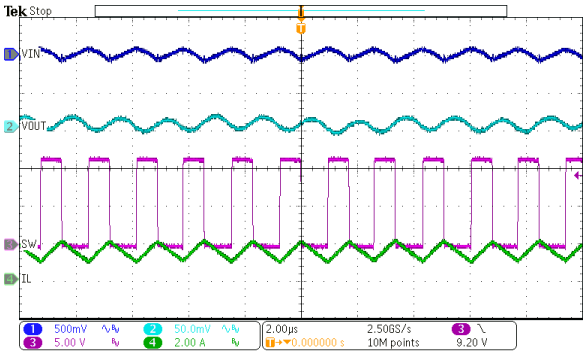


Figure-34. Output Voltage Ripple, I_{OUT} = 1.5A

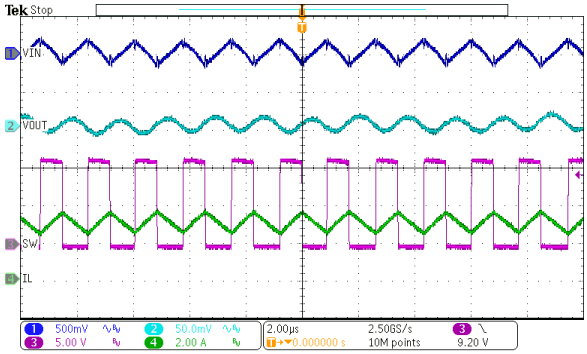


Figure-35. Output Voltage Ripple, I_{OUT} = 3A

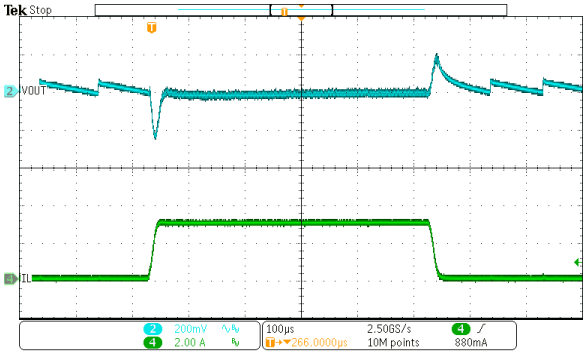


Figure-36. Load Transient, I_{OUT} = 0A-3A, 250mA/µs

Test Conditions: V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C (unless otherwise noted)

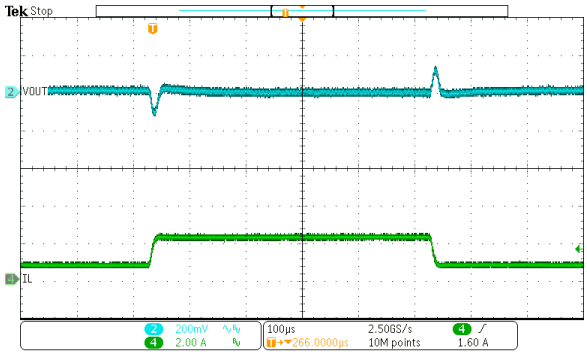


Figure-37. Load Transient Response, I_{OUT} = 0.5A-1.5A, 250mA/µs

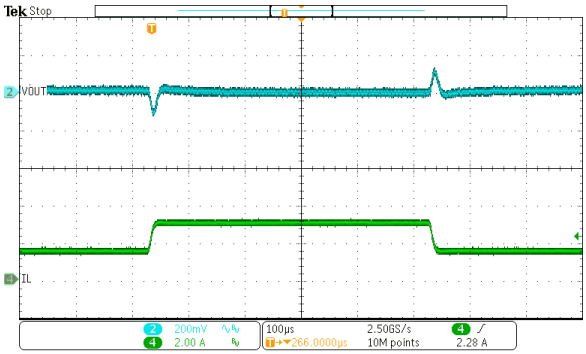


Figure-38. Load Transient Response, I_{OUT} = 1.5A-3A, 250mA/µs

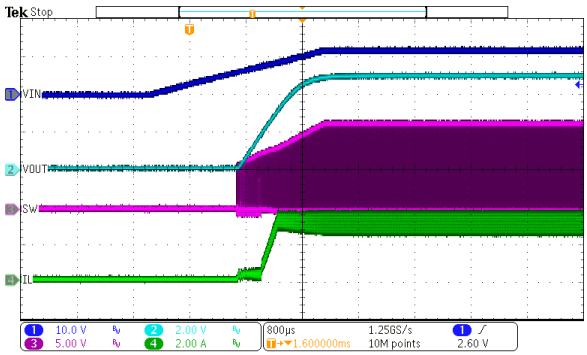


Figure-39. V_{IN} Start-Up, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A

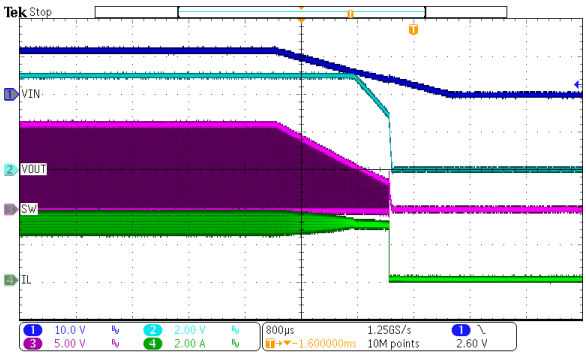


Figure-40. V_{IN}Shut-Down, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A

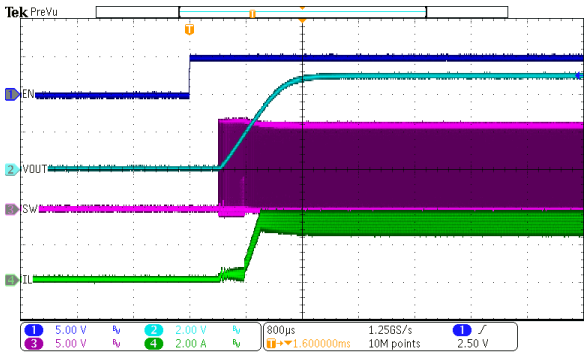


Figure-41. EN Start-Up, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A

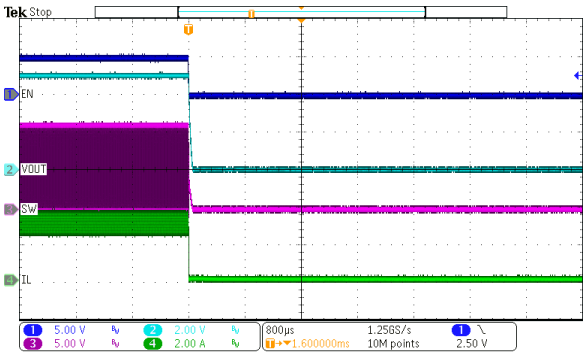
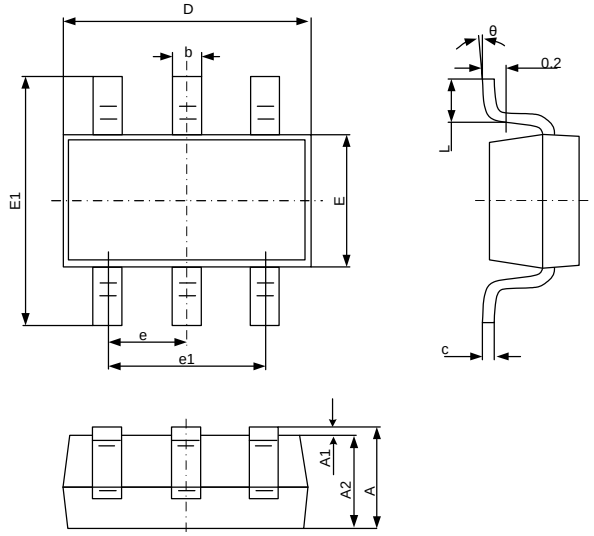


Figure-42. EN Shut-Down, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A

PACKAGE DIMENSION

SOT23-6



Symbol	Dimensions (Millimeters)		Dimensions (Inches)	
	Min.	Max.	Min.	Max.
A	-	1.350	-	0.053
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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