

40V N-Channel Power MOSFET

BV_{DSS}	40V	R_{DS(ON)_MAX}	1.24mΩ
I_{D_MAX}	288A	Q_{g_TYP}	69nC

Feature

- Maximum R_{DS(ON)} < 1.24mΩ at V_{GS} = 10V
- Maximum R_{DS(ON)} < 1.48mΩ at V_{GS} = 7V
- N channel MOSFET - Standard Level
- Excellent FoM (R_{DS(on)} × Qg)
- 175°C operating temperature
- 100% Avalanche & Rg tested
- Package with Side Wettable Flanks (SWF) for automated optical solder inspection (AOI)
- AEC-Q101 qualified and PPAP capable
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

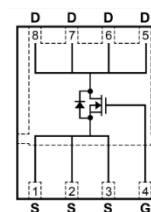
Mechanical Data

- Case : Advanced DFN5060SW-8L Package (Patented)
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.1056 gram

Application

- DC-DC Converters
- Motor Drivers
- Automotive Applications

DFN5060SW-8L



Top side view

Absolute Maximum Ratings (T_J=25°C unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V _{DS}	40	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain Current ⁽¹⁾	T _C =25°C	I _D	288	A
	T _C =75°C		235	
	T _C =100°C		203	
Pulsed Drain Current	T _C =25°C, t _p ≤100us	I _{DM}	1282	
Power Dissipation	T _C =25°C	P _D	195	W
	T _C =75°C		130	
	T _C =100°C		97	

PARAMETER		SYMBOL	VALUE	UNIT
Continuous Drain Current ⁽¹⁾	T _A =25°C	I _D	46.1	A
	T _A =75°C		37.6	
	T _A =100°C		32.6	
Power Dissipation	T _A =25°C	P _D	5	W
	T _A =75°C		3.3	
	T _A =100°C		2.5	
Body Diode Continuous Current ⁽¹⁾	T _C =25°C	I _S	191	A
Body Diode Pulse Current	T _C =25°C, t _p ≤100us	I _{SM}	1282	
Single Pulse Avalanche Current ⁽²⁾		I _{AS}	56	
Single Pulse Avalanche Energy	I _{AS} =28A, limited by T _{J_MAX}	E _{AS}	624	mJ
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~175	°C

(1).Thermal Characteristics

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Thermal Resistance	Junction to Ambient ⁽³⁾	R _{θJA}	—	30	—	°C/W
	Junction to Case	R _{θJC}	—	0.59	0.77	
	Junction to Case _(TOP)	R _{θJC_top}	—	—	17	

(2). Notes :

- (3). The maximum continuous current of chip capability is calculated by maximum junction temperature and thermal resistance, and it will vary depending on the application and environment.
- (4). L=0.1mH, 100% test in production.
- (5). Surface mounted on 4 layers (2s2p) FR4 PCB defined in accordance with JESD51-5/ JESD51-7.

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =1mA	40	—	—	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.2	2.7	3.2	
Drain-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	—	0.95	1.24	mΩ
		V _{GS} =7V, I _D =15A	—	1.14	1.48	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	—	—	1	μA
		V _{DS} =40V, V _{GS} =0V, T _J =125°C ⁽⁴⁾	—	—	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	—	—	±100	nA
Gate Resistance	R _g	f =1MHz	—	1	—	Ω
Transfer characteristics ⁽⁴⁾	g _{fs}	V _{DS} =5V, I _D =30A	—	150	—	S
Dynamic Characteristics ⁽⁴⁾						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHz	—	4490	5837	pF
Output Capacitance	C _{oss}		—	1360	1768	
Reverse Transfer Capacitance	C _{rss}		—	100	150	
Output Charge	Q _{oss}	V _{DD} =20V, V _{GS} =0V	—	49	—	nC
Total Gate Charge	Q _g	V _{DD} =20V, I _D =30A, V _{GS} =0~10V	—	69	90	
Gate-Source Charge	Q _{gs}		—	18	23	
Gate-Drain Charge	Q _{gd}		—	13	20	
Threshold Gate Charge	Q _{g(th)}		—	12	—	
Switching Charge	Q _{sw}		—	19	—	
Gate Plateau Voltage	V _{plateau}		—	4.1	—	V
Total Gate Charge, sync. FET	Q _{g(sync)}	V _{DD} =0.1V, I _D =30A, V _{GS} =0~10V	—	56	—	nC
Turn-On Delay Time	t _{d(on)}	V _{DD} =20V, V _{GS} =10V, I _D =30A, R _G =3Ω	—	17	—	ns
Rise Time	t _r		—	8	—	
Turn-Off Delay Time	t _{d(off)}		—	42	—	
Fall Time	t _f		—	11	—	
Body Diode						
Diode Forward Voltage	V _{SD}	I _S =30A, V _{GS} =0V	—	0.8	0.96	V
Reverse Recovery Charge ⁽⁴⁾	Q _{rr}	I _S =30A, di/dt=100A/μs	—	30	—	nC
Reverse Recovery Time ⁽⁴⁾	T _{rr}		—	36	—	ns

Notes :

(6). Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

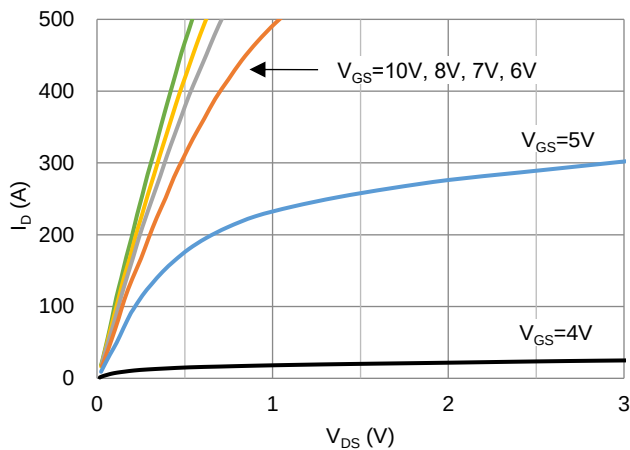


Fig.1 Output Characteristics

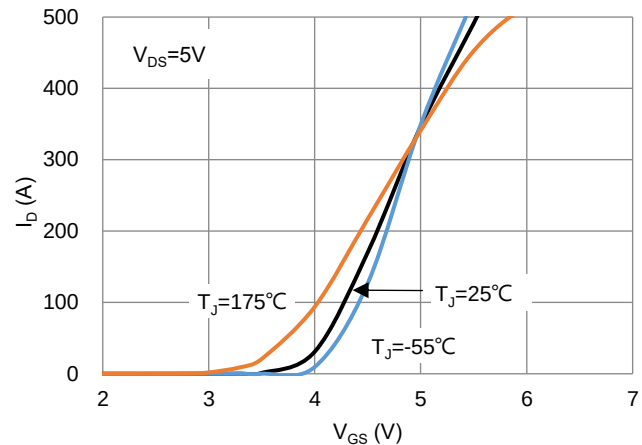


Fig.2 Transfer Characteristics

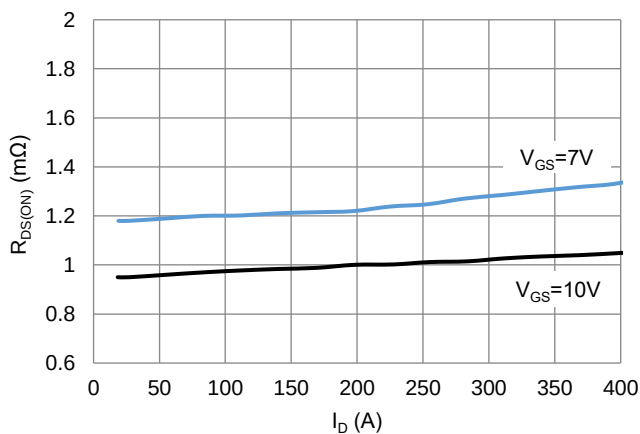


Fig.3 On-Resistance vs. Drain Current

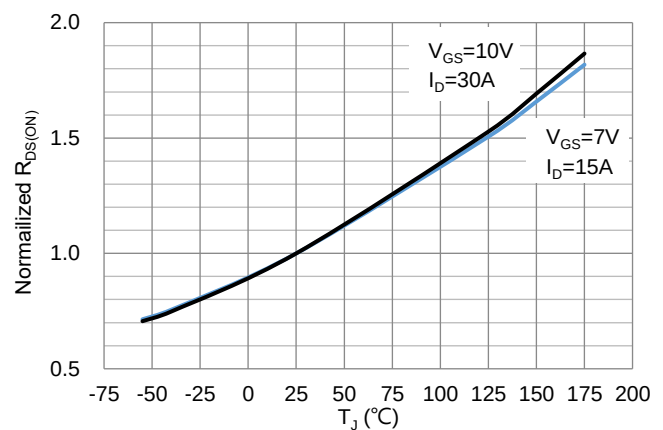


Fig.4 On-Resistance vs. Junction temperature

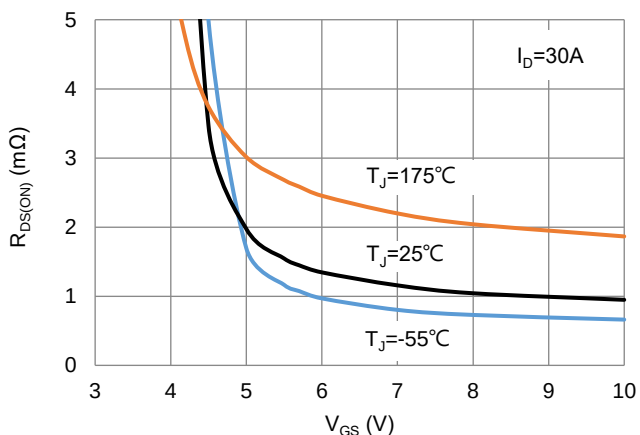


Fig.5 On-Resistance vs. Gate Voltage

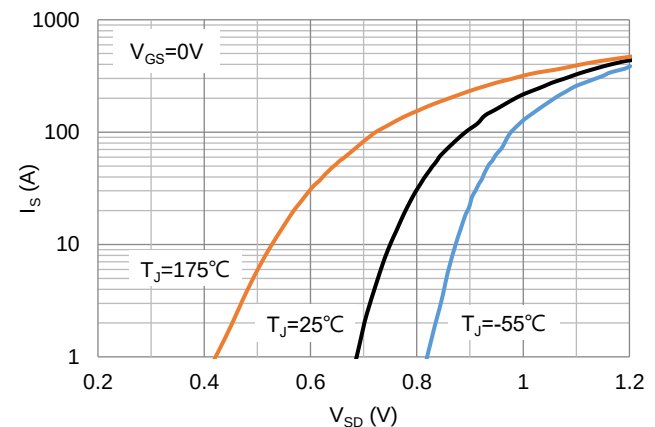


Fig.6 Body Diode Characteristics

TYPICAL CHARACTERISTIC CURVES

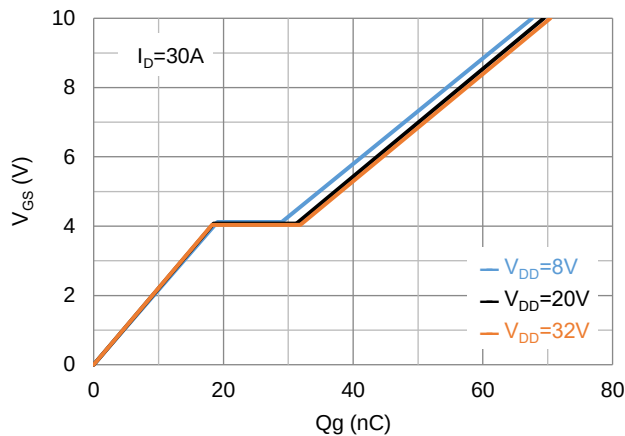


Fig.7 Gate-Charge Characteristics

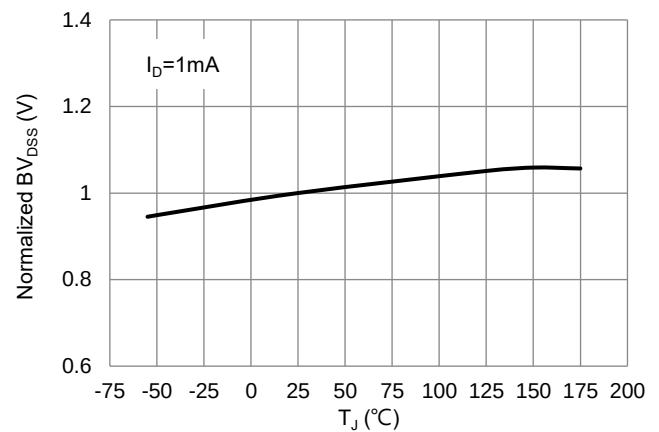


Fig.8 Breakdown Voltage vs. Junction Temperature

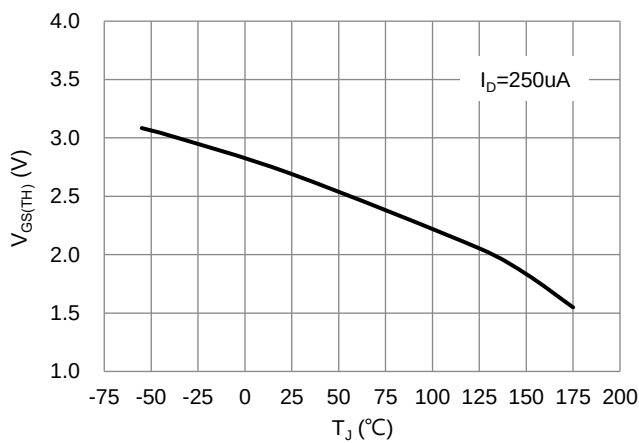


Fig.9 Threshold Voltage vs. Junction Temperature

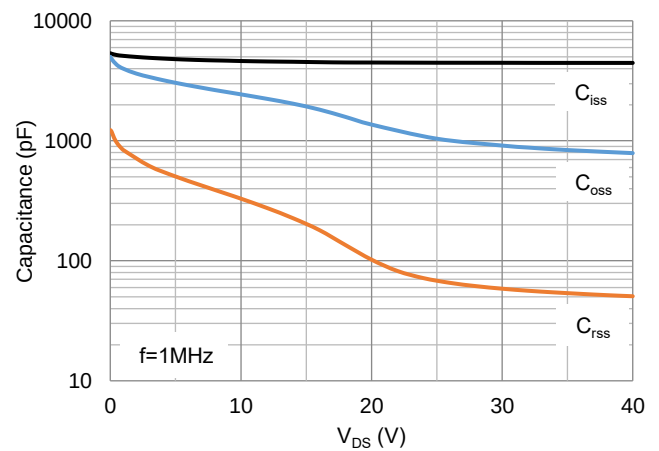


Fig.10 Capacitance vs. Drain-Source Voltage

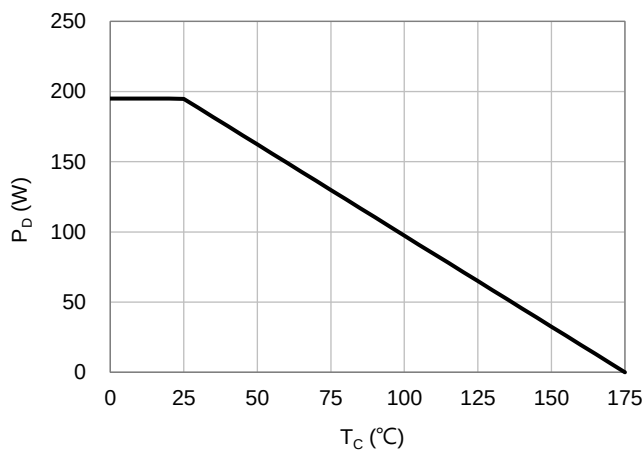


Fig.11 Power Dissipation vs. Case Temperature

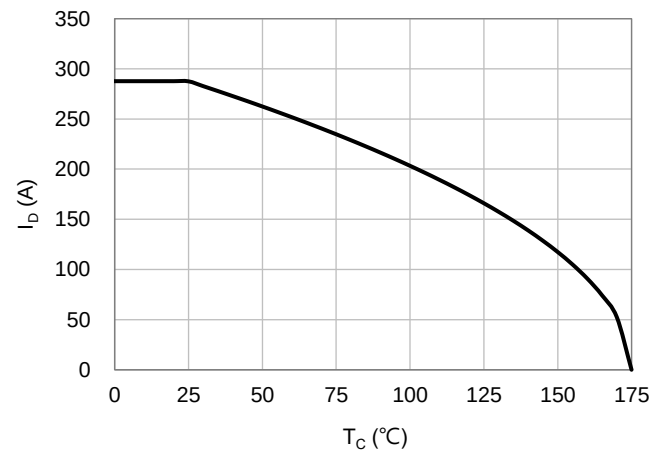


Fig.12 Drain Current vs. Case Temperature

TYPICAL CHARACTERISTIC CURVES

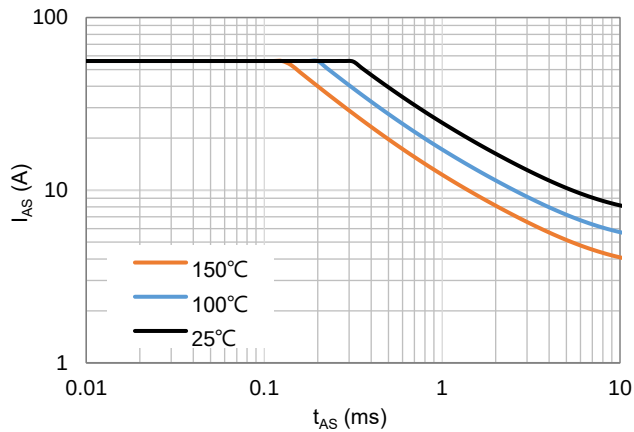


Fig.13 Avalanche characteristics

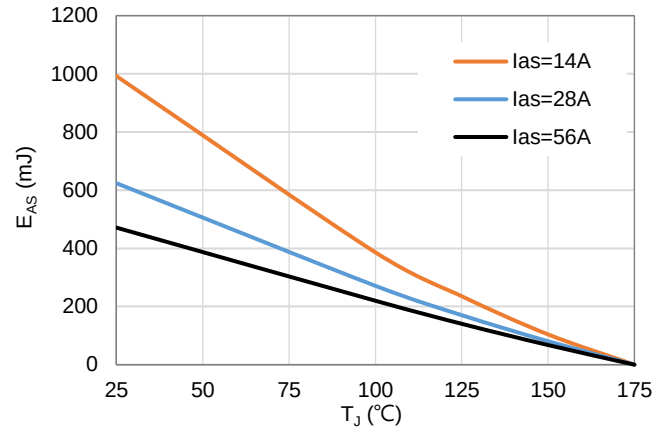


Fig.14 Avalanche Energy

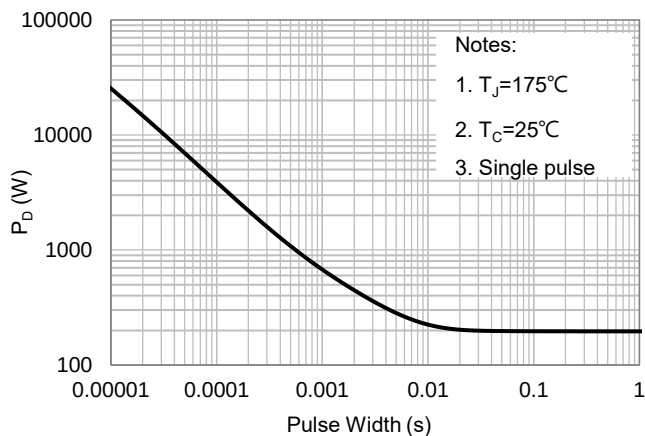


Fig.15 Power Dissipation vs. Pulse Width

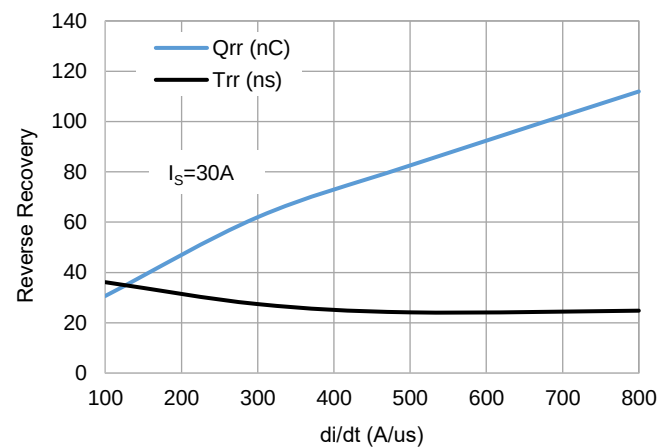


Fig.16 Body Diode Reverse Recovery characteristics

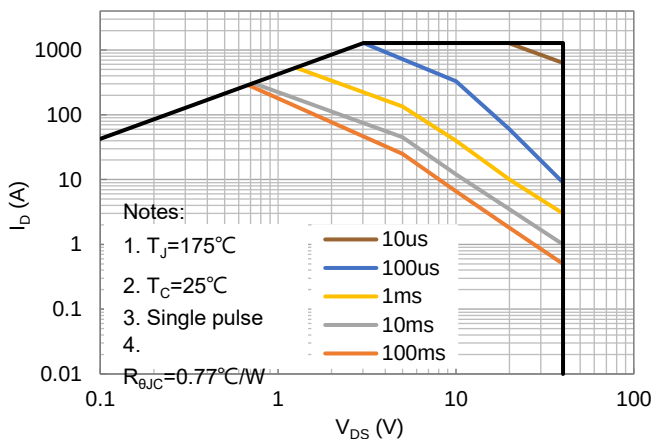


Fig.17 Maximum Safe Operating Area

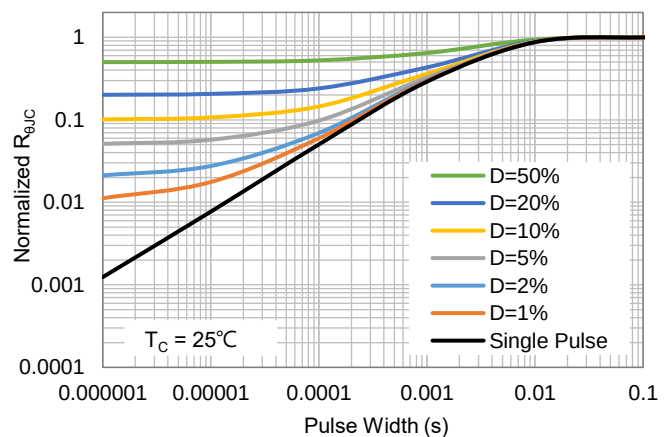


Fig.18 Normalized Thermal Impedance

TEST CIRCUITS AND WAVEFORMS

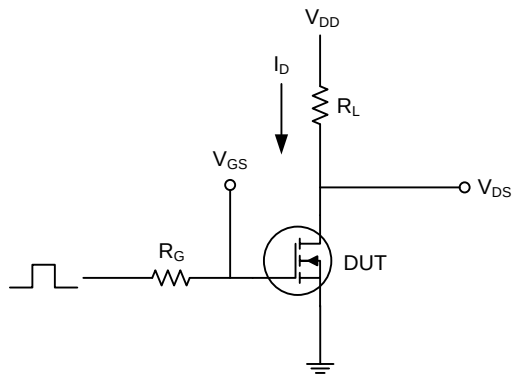


Fig.19 Switching Time Test Circuit

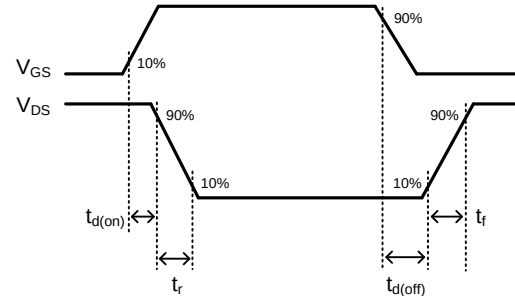


Fig.20 Switching Time Waveform

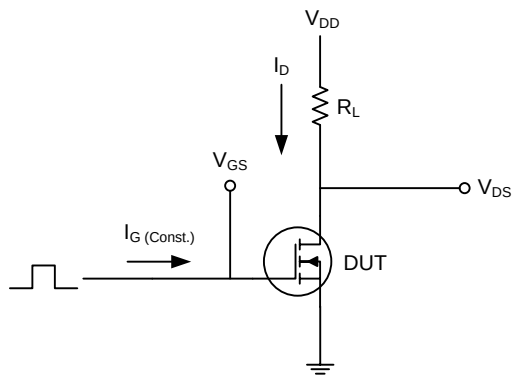


Fig.21 Gate Charge Test Circuit

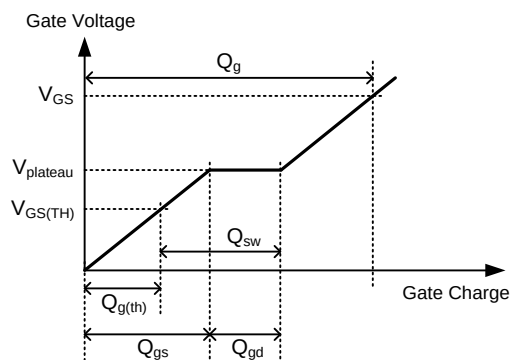


Fig.22 Gate Charge Waveform

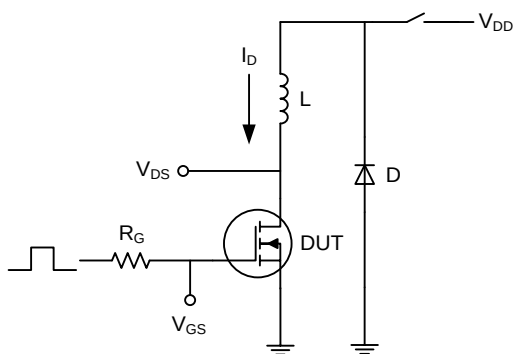


Fig.23 Avalanche Test Circuit

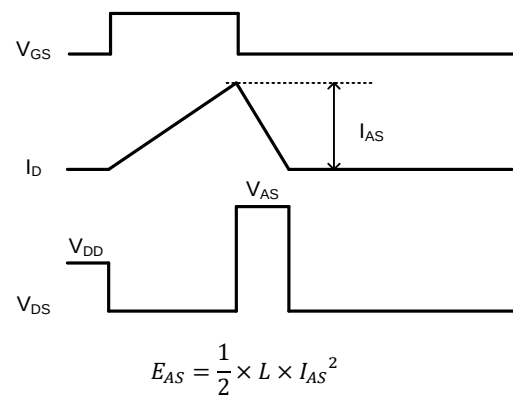
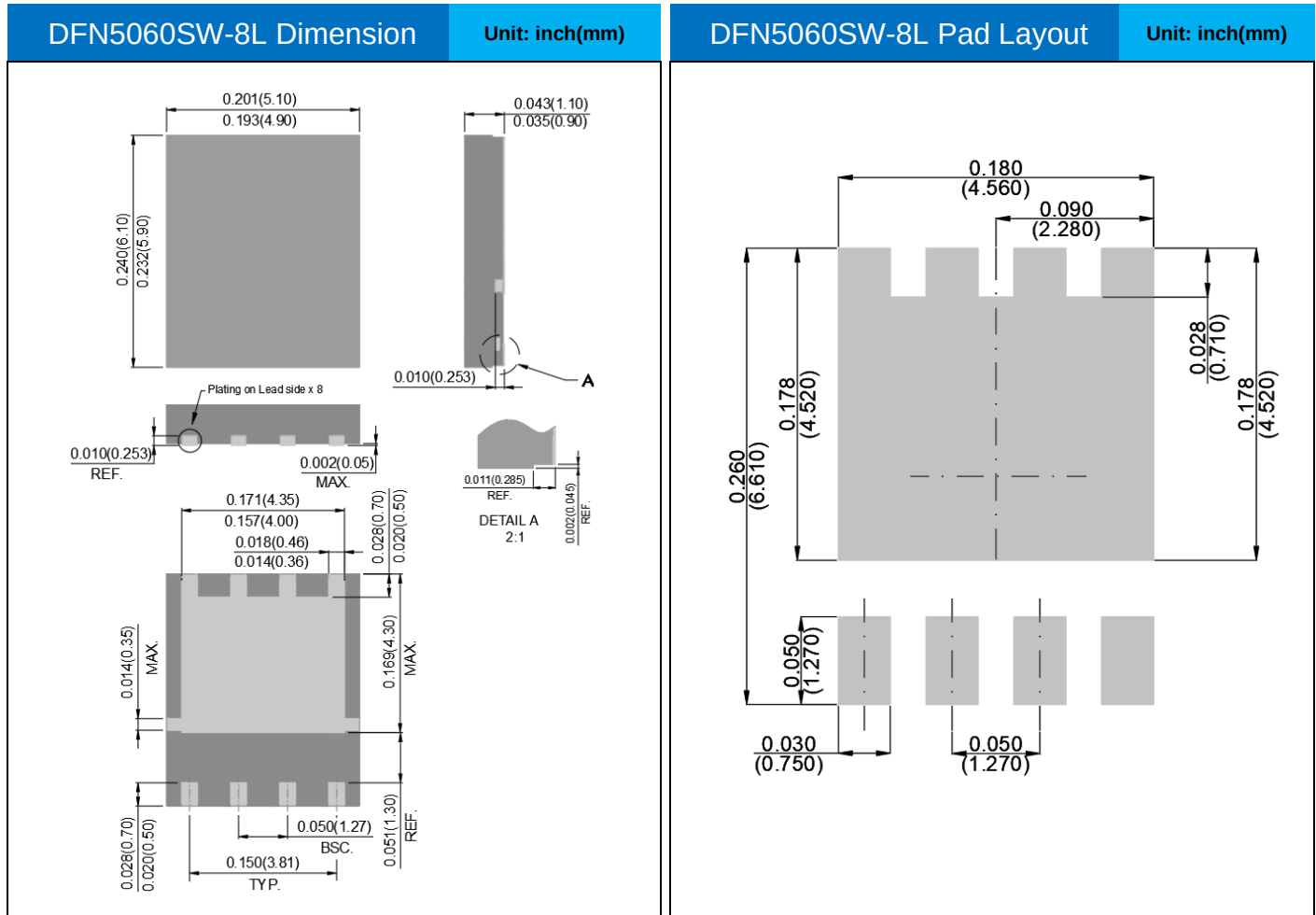


Fig.24 Avalanche Waveform

Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PSMWF011N04NS3-AU	DFN5060SW-8L	3K pcs / 13" reel	011N04NS

Packaging & Layout Information



Marking Diagram

PJ 011N04NS YWLL x	Y = Year Code
	W = Week Code (A~Z)
	LL = Lot Code (00~99)
	x = Production Line Code

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