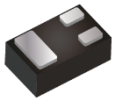
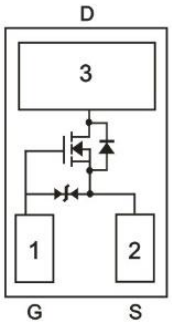
PJQ1908

50V N-Channel Enhancement Mode MOSFET

Voltage	50 V	Current	500mA

DFN1006-3L





Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@500mA<1.45Ω
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@200mA<1.95Ω
- $R_{DS(ON)}$, V_{GS}@2.5V, I_D@100mA<4Ω
- $R_{DS(ON)}$, V_{GS}@1.8V, I_D@10mA<6Ω
- Advanced Trench Process Technology
- ESD Protected 2KV HBM
- Specially Designed for Switch Load
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN1006-3L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0007 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current(Note 4)		I_D	500	mA
Pulsed Drain Current(Note 1)		I_{DM}	1200	
Power Dissipation	T_A=25°C	P_D	900	mW
	Derate above 25°C		7.2	mW/°C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Thermal Resistance - Junction to Ambient, t<10s(Note 5)		$R_{\theta JA}$	139	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.5	0.86	1	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=500mA	-	1.2	1.45	Ω
		V_{GS}=4.5V, I_D=200mA	-	1.3	1.95	
		V_{GS}=2.5V, I_D=100mA	-	1.7	4	
		V_{GS}=1.8V, I_D=10mA	-	3	6	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±10	
Dynamic(Note 6)						
Total Gate Charge	Q_g	V_{DS}=25V, I_D=500mA, V_{GS}=4.5V(Note 1,2)	-	0.95	-	nC
Gate-Source Charge	Q_{gs}		-	0.34	-	
Gate-Drain Charge	Q_{gd}		-	0.32	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	36	-	pF
Output Capacitance	Coss		-	11	-	
Reverse Transfer Capacitance	Crss		-	6.6	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=25V, I_D=500mA, V_{GS}=10V, R_G=3Ω(Note 1,2)	-	2.3	-	ns
Turn-On Rise Time	t_r		-	20	-	
Turn-Off Delay Time	$td_{(off)}$		-	7	-	
Turn-Off Fall Time	t_f		-	20	-	
Drain-Source Diode						
Diode Forward Current	I_S	---	-	-	500	mA
Diode Forward Voltage	V_{SD}	I_S=500mA, V_{GS}=0V	-	0.9	1.5	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch^2 with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

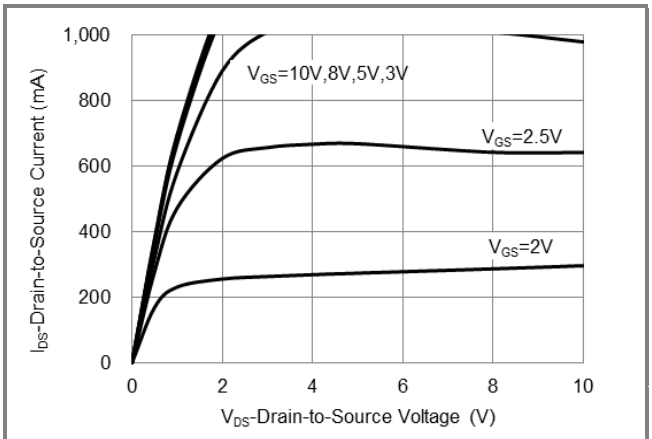

Fig.1 Output Characteristics

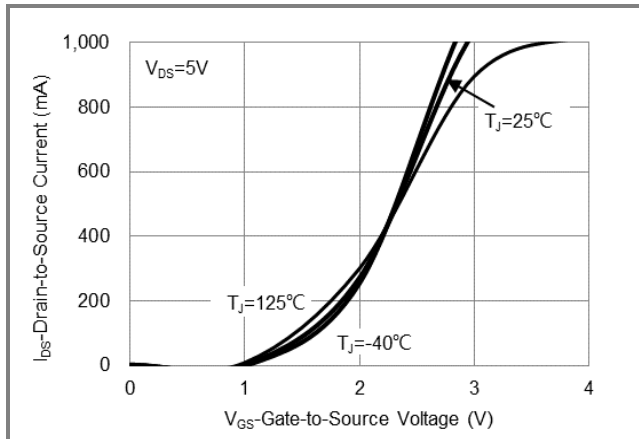

Fig.2 Transfer Characteristics

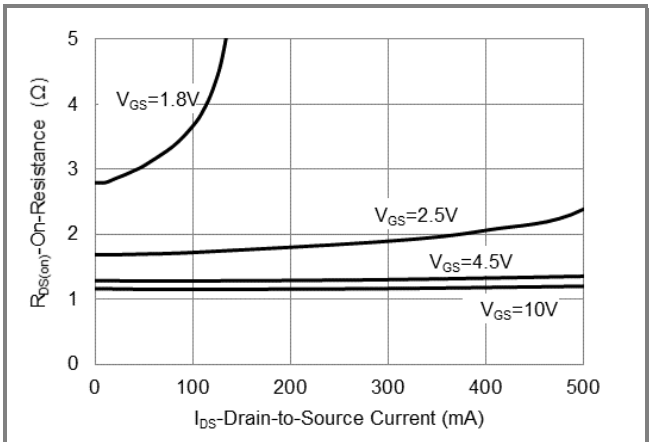

Fig.3 On-Resistance vs. Drain Current

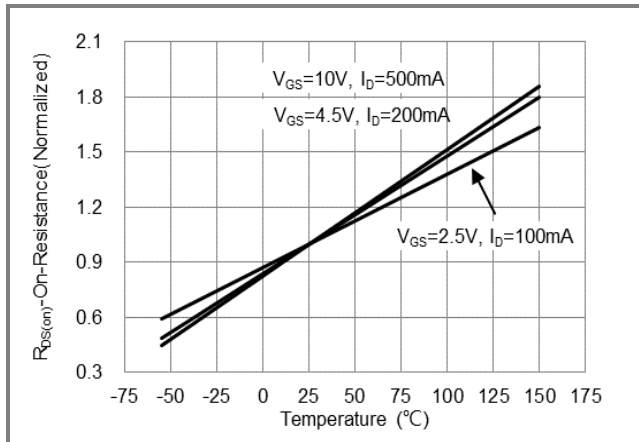

Fig.4 On-Resistance vs. Junction temperature

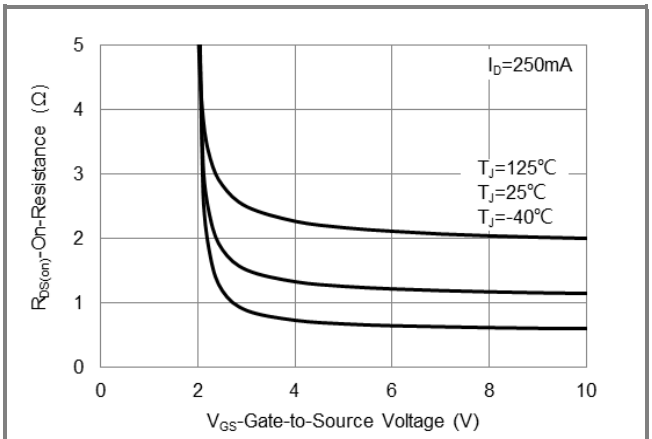

Fig.5 On-Resistance Variation with V_{GS}

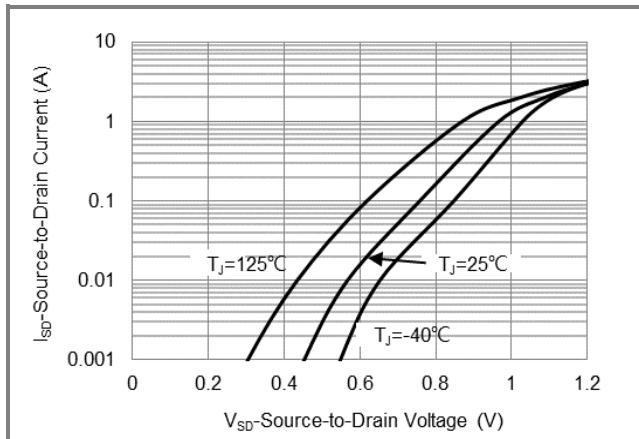

Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

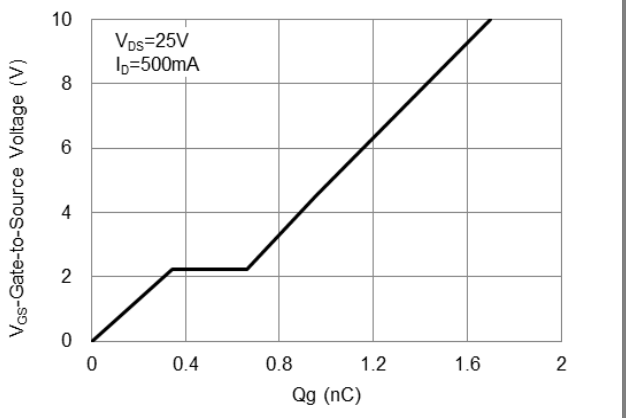


Fig.7 Gate-Charge Characteristics

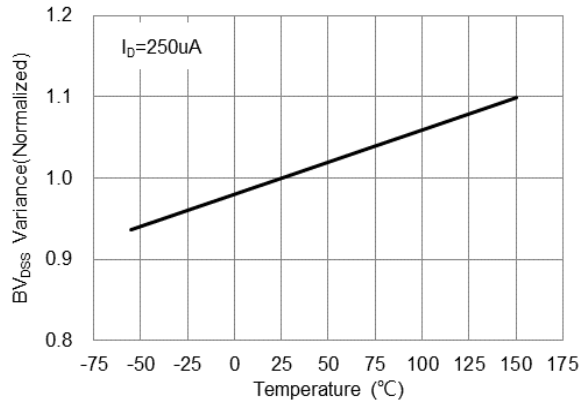


Fig.8 Breakdown Voltage Variation vs. Temperature

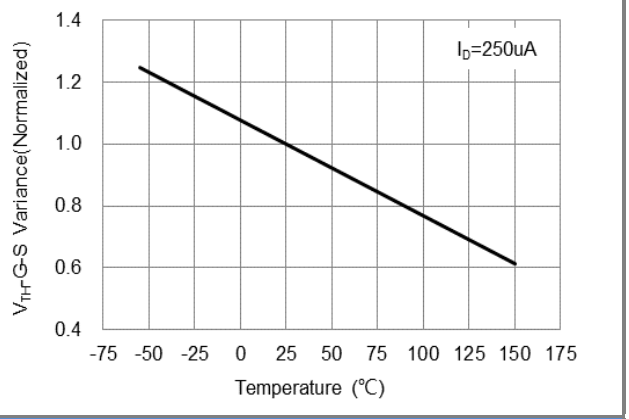


Fig.9 Threshold Voltage Variation with Temperature

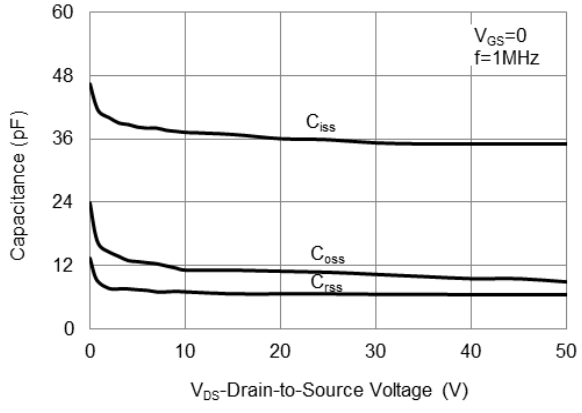


Fig.10 Capacitance vs. Drain-Source Voltage

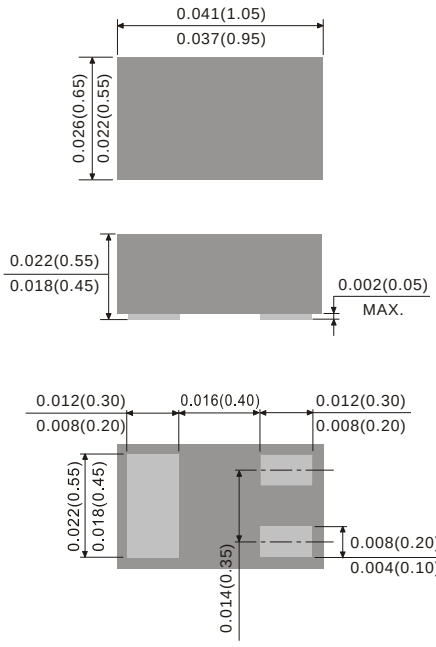
PJQ1908

Product and Packing Information

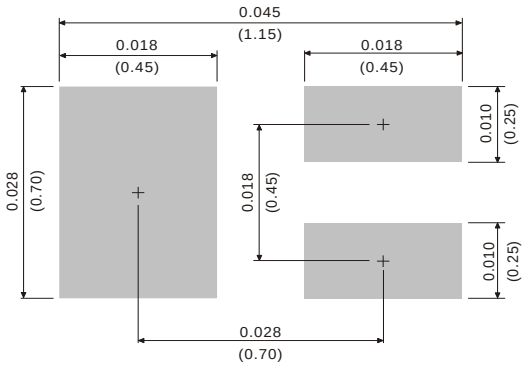
Part No.	Package Type	Packing Type	Marking
PJQ1908	DFN1006-3L	10K pcs / 7” reel	8

Packaging Information & Mounting Pad Layout

DFN1006-3L Dimension — Unit: inch(mm)



DFN1006-3L Pad Layout — Unit: inch(mm)



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